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The Chairman's Column

To Members of the PGEC

By the time you read this you should have received the special newsletter which I sent to you in January, and I hope that you have taken the few minutes required to approve our amended constitution. While a request for more money is never pleasant, I'm sure that you'll agree with me that as PGEC members we're receiving a good return on the new $4 membership fee.

There have been a number of other developments about which you should be appraised, and I shall take these up chronologically, beginning with an executive committee meeting which was held during WESCON last August.

The Abstracting Service—Our contract for abstracting services with Mr. Geoffrey Knight, Jr., was extended for another year at a cost not to exceed $6,000. It had become apparent in August that we would not receive support from NJCC in the abstracting business and, while the PGEC does not intend to underwrite the project indefinitely, it did not seem prudent to let the program die on its feet after the first year's activity. So we're in the abstracting business at least until September, but in the meantime we're seeking other means of keeping the effort afloat at reduced or no cost to PGEC.

The National Joint Computer Committee—The charter of the NJCC has been the subject of much discussion and consideration over the past several months and, indeed, to one extent or another since the day the organization went into operation. Briefly, the NJCC is comprised of the PGEC, the ACM, and the AIEE Committee on Computing Devices. Its sole original and present purpose of existence was for the origination and organization of two computer conferences each year, now well established, and known to us all as EJCC and WJCC (Eastern and Western Joint Computer Conferences). Beyond this NJCC had (and has) no teeth or power to act on any question not originally delegated to it by the three sponsoring societies. Returning each time to the parent societies for authorization to act on any particular question is cumbersome and, in light of timing required sometimes is impossible. Thus, the NJCC has been due for an overhaul, and the process was begun in three specific meetings held in Boston during the recent EJCC: an administrative committee meeting of the PGEC on November 30th, an informal "off-the-record" meeting of an enlarged NJCC on December 1, and a formal scheduled meeting of the NJCC on December 2. I am sure there were numerous other meetings as well called extemporaneously in the halls and various rooms of the Statler.

The Administrative Committee of the PGEC, in considering the question at its meeting of November 30, passed a resolution stating its position. The PGEC proposed, in essence, that the NJCC

1) be the vehicle for representation of the United States in the IFIPS (International Federation of Information Processing Societies).
2) provide unified domestic representation of the information processing fraternity.
3) promote education in the computer arts (*i.e.*, SE-NEWS), sponsor and coordinate meetings and symposia, and assume other tasks which might normally be identified with a central information-processing society, such as speakers bureaus, etc.
4) be dissolved . . . and reorganized under a new name such as, but not necessarily, American Federation of Information Processing Societies and, as such,
   a) have *vested* authority and responsibility as well as financial autonomy.
   b) become a society of societies (as opposed to a suggested society of members), with membership open to all organizations of professional stature which have a legitimate and significant claim to identification with the field of information processing, such as SIAM, NOMA, Simulation Council, and perhaps our sister Professional Groups PGIT and PGAC, as well as ACM and AIEE. No particular recommendation was made at this time as to the definition of possible grades (levels) of society membership.

PGEC's position, set forth in both the December 1 and December 2 meetings of the NJCC, was found to concur closely with the position of the AIEE and eventually with that of the ACM, since the NJCC did finally resolve on December 2 that it should be reorganized, and broadly at least within the framework of the PGEC proposal. Responsibility for initiating the process of reorganization was given to the NJCC Executive Committee, composed of Dr. Harry Goode who is present NJCC Chairman, and the chairmen of the three societies (ACM, AIEE, PGEC).

International Federation of Information Processing Societies—As you may know, out of the UNESCO-sponsored International Conference on Information Processing held in Paris last June, the IFIPS was formed. It is the charter of this society to which NJCC (or its successor) is adhering in representation of the United States. The ACM and the AIEE ratified the statutes earlier this fall, while the PGEC Administrative Committee gave its approval in November. The IRE Executive Committee at its regularly scheduled meeting held on December 15th gave IRE approval, underscoring the fact that it is the IRE represented in the IFIPS—not the PGEC—but that the IRE has appointed PGEC to be its representative.

The Constitution and Bylaws—Again, I hope that you have voted your approval of the amended constitution which was sent to you in January. The changes reflect continuing growth of the PGEC in both number and responsibility and, once implemented, will assist the Administrative Committee greatly in discharging its tasks.

I want to extend my personal thanks to J. Claude LaPointe who, as Chairman of the Constitution and Bylaws Committee, spent a great many hours reworking our constitution with recommendations of his own and coordinating suggestions from the Administrative Committee and Headquarters. Claude resigned his post following submission of his final manuscript, and the work of the committee will be picked up by Charles Rosenthal.

Richard O. Endres
Chairman, 1959–1960

Transistor Pulse Circuits for 160-MC Clock Rates*

W. J. GIGUERE†, J. H. JAMISON†, AND J. C. NOLL†

Part I—Pulse Regeneration

W. J. GIGUERE AND J. H. JAMISON

Summary—This paper consists of two parts. Part I, by Giguere and Jamison, discusses transistor circuits capable of regenerating 6.25-mμsec pulses at a 160-mc bit rate. Part II, by Noll, discusses techniques for multiplexing 16 digital signals with a 10-mc clock rate into a single signal with a 160-mc clock rate.

Two methods of performing the regeneration function are presented. One method consists of dc level restoration for recognition of the signal and constant current coincident circuitry for the reconstruction of the pulses. The second method consists of operating on changes in the signal for pulse recognition and the use of a bistable circuit for pulse reconstruction. Timing in the second case is obtained by a constant current coincidence gate.

Parallel-to-serial multiplexing techniques have been developed to combine sixteen parallel 10-mc clock-rate signals into a 160-mc clock-rate pulse train. The sixteen synchronous signals are applied to sixteen AND gates along with a 10-mc narrow gate pulse. The space separations of the resulting regenerated and timed AND gate output pulses is converted to time separation with only a small amount of signal loss. This is done by injecting the pulses at sixteen equally separated points on a broad-band delay line. Methods have been developed to reduce spurious responses resulting from multiple reflections on the delay line.

The current mode transistor AND gates are suitable for AND/OR functions for individual 4-mμsec logic. The multiplexer may also be used as a piece of test equipment to generate repetitive 16-bit binary words with a 10-mc frame rate.

Introduction

THE circuits to be described here are the result of preliminary exploratory development into high-speed pulse code modulation. Particularly, the aim has been to discover methods of performing the functions necessary for pulse regeneration at a 160-mc bit rate with semiconductor devices.

The 160-mc pulse repetition rate prevents the use of many of the standbys of pulse regeneration at slower speeds. For example, it has not yet been possible to devise a blocking oscillator or similar monostable device for the reconstruction of pulses at these rates.

Three specific functions necessary for regeneration will be discussed: 1) recognition of pulse information that has been ac coupled through a transmission system, 2) reconstruction of a pulse once it has been recognized as one, and 3) retiming of a pulse so that it occupies its correct position in a time slot.

The transistors used in the circuit make a balanced type signal desirable to achieve a high-level output from the regenerator. The output of a balanced type binary code generator consists of either positive "one" or negative "zero" pulses as the two binary alternatives instead of the more common pulse and space alternatives. A feature of this type of signal is that both "ones" and "zeros" contain timing information. This will aid in extracting the 160-mc frequency for the self-timing of repeaters because of the more constant 160-mc component which can be derived from a signal with variable pulse patterns.

In anticipation of the final results, Fig. 1 shows the regenerated pulse train of three widely differing pulse patterns as displayed on an electrical stroboscope designed by Goodall.[1] In these photographs, the time represented between adjacent ones or adjacent zeros is 6.25 mμsec.

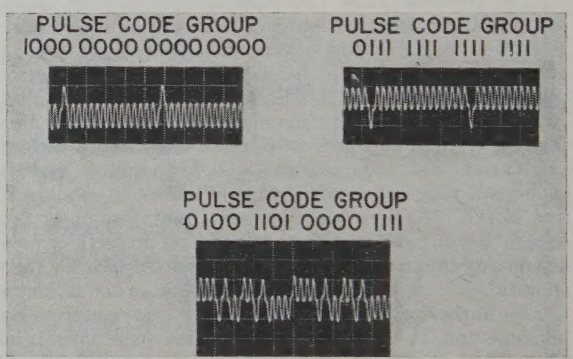

Fig. 1—Regenerated pulse patterns of 160-mc PCM code groups repeating at a 10-mc rate. Strobescope time scale represents 20 mμsec per major division.

Two methods of recognition and regeneration of a pulse train will be described. The methods differ mainly in the manner of pulse recognition. One method involves the determination of a zero from a one on the basis of its relation to a specific dc voltage level. The other method recognizes transitions from zero to one or one to zero and operates on these changes.

Method 1—DC Level Recognition

DC Restorer

The low-frequency cutoff of a transmission system imposes a changing dc level on the pulse train that depends on the pulse pattern.

The top pattern in Fig. 2 shows the effect of this level change with a boxcar representation of differing pulse patterns in a system with a rather high low-frequency

* Manuscript received by PGEC, July 23, 1959. This paper was presented at the 1959 Solid-State Circuits Conf., University of Pennsylvania, Philadelphia, Pa.; February 12–13, 1959.

† Bell Telephone Labs., Inc., Murray Hill, N. J.

[1] W. M. Goodall, "An Electrical Stroboscope for Pico Second Pulses," Bell Telephone Labs., Inc., Holmdel, N. J., to be published.

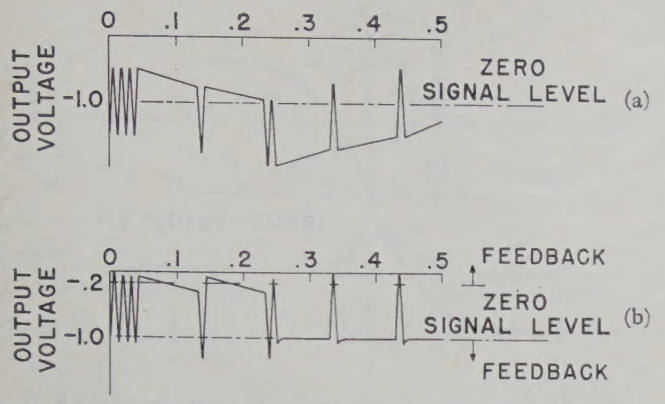

Fig. 2—(a) DC output with high low-frequency cutoff time. (b) DC output with dc restoration. (Time axis in microseconds.)

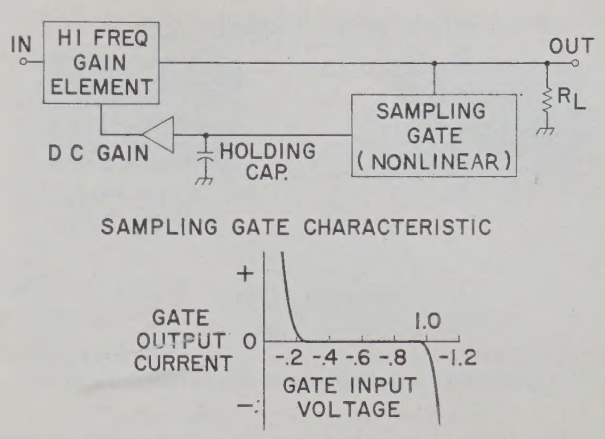

Fig. 3—Nonlinear dc restorer.

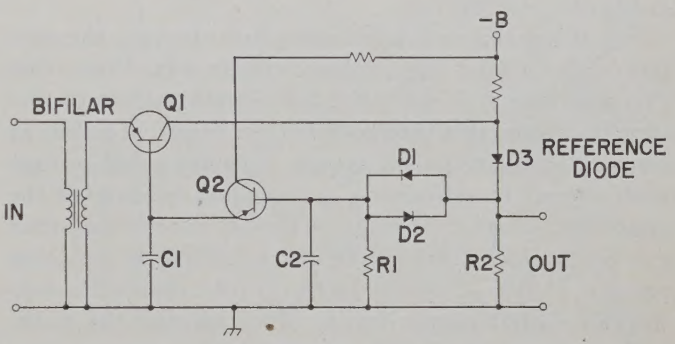

Fig. 4—Nonlinear dc restorer schematic.

cutoff. This shows that if pulses were to be distinguished from spaces on the basis of their polarity with respect to a specified dc level, conditions would occur that could prohibit recognition in the presence of very little noise. The bottom pattern in Fig. 2 shows the same pulse pattern with the original dc restored to the signal so that recognition of the pulses is possible around a dc level. It is obvious that transitions from one to zero and zero to one are not appreciably affected provided that only the lowest frequencies are lost from the spectrum.

Fig. 3 is a block diagram that shows the means by which the peaks of the pulse train are used to perform the dc restoring function.

The pulse code signal is amplified and direct-coupled to a circuit consisting of two high-speed silicon diodes connected in parallel with opposing conductivity. These diodes provide a limiting range within which the signal is confined. Normally, the signal amplitude is such that it causes a small amount of diode conduction at the peaks of the ones and zeros. An unbalance in the conduction of the limiting diodes produces a correcting bias voltage that changes the dc voltage level at the amplifier output to cause equal conduction of the diodes. This provides that a signal composed of many ones and few zeros will be held within the same range as a signal with many zeros and few ones. This allows the determination of ones from zeros around a dc threshold at the center of this voltage range. The response time of the dc correcting circuitry is adjusted to compensate for the pulse pattern dc drift caused by the low-frequency cutoff of the system.

Fig. 4 is a schematic of this type of restorer. Q_1 is a high-frequency diffused-base transistor. This transistor operates in a linear region with its bias controlled by the conduction of a low-frequency amplifier Q_2. The high-speed silicon diodes D_1 and D_2 allow the peaks of the pulses to charge C_2. The average conduction of D_1 and D_2 depends on the pulse pattern and determines the conduction of Q_2. D_3 is a voltage reference diode which acts as a battery and is used as a dc path from the signal to a lower operating voltage level. C_2 and the input impedance of the low-frequency amplifier determine the response of the dc restorer to changes in the pulse pattern. This time constant is set to follow the low-frequency cutoff of the transmission system preceding the dc restorer. The output level of the dc restorer is adjusted to cause very little signal degradation from peak charge transfer through the high-speed sampling diodes. The low-frequency transistor amplifies the net charge to maintain and correct for dc level changes. A balanced version of this dc restorer is direct-coupled to a regenerative timing gate.

Regenerative Timing Gate

Fig. 5 shows a balanced transistor gate in which both regeneration of the signal and the timing of the pulses are done at the same time. The emitters of the gate transistors are driven by a 160-mc, 3.2-mμsec half sine wave timing pulse from Q_3. The collector of Q_3 appears as a constant current source to the emitters of the gate transistors. A sufficient voltage difference between the bases of Q_1 and Q_2 will cause conduction through the transistor with the more negative base when the timing pulse is applied. The conduction of Q_3 determines the conduction period of Q_1 or Q_2, as well as the time of conduction and the maximum current pulse during conduction. The gate transistor outputs are combined in a balanced-to-unbalanced output transformer[2] so that conduction of one transistor forms ones; conduction of

[2] C. L. Ruthroff, "Some broad-band transformers," PROC. IRE, vol. 47, pp. 1337–1342; August, 1959.

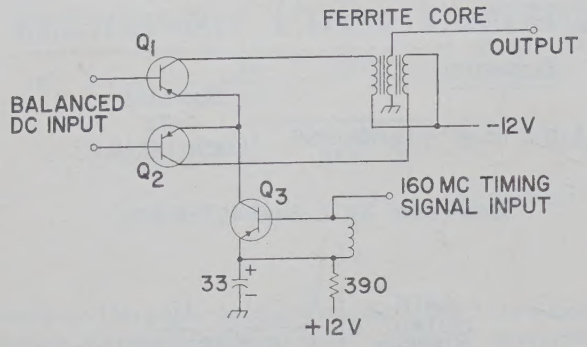

Fig. 5—160-mc regenerative timing gate schematic.

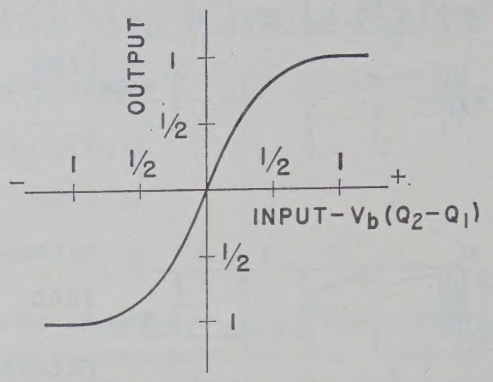

Fig. 6—Normalized characteristic for partial regenerator.

the other forms zeros. The output transformer consists of a trifilar wound coil on a ferrite core; its bandwidth is in the order of 800 mc.

Fig. 6 is a characteristic of the gate showing the output with varying base voltage differences. From this characteristic, it is seen that the output pattern of this type of regenerator produces distinct negative pulses as zeros and positive pulses as ones. This has an advantage with respect to self-timing of repeaters because of the relatively constant amount of timing information that can be obtained from the signal regardless of the pulse pattern. It also allows the formation of a four-volt peak-to-peak output signal into 50 ohms because the push-pull arrangement of the gate requires less average conduction of each transistor.

Fig. 7 shows the combination of a balanced version of the dc restorer previously described and the regenerative gate to provide regeneration and timing. In this circuit, Q_1 and Q_2 are high frequency diffused-base transistors. The bias of these transistors is adjusted by the conduction of the low-frequency transistors Q_3 and Q_4. C_2 and C_3 are the averaging capacitors, and diodes D_3 and D_4 form the peak sampling means. Voltage reference diodes are again used to direct-couple the signal to a lower average voltage level.

This completes one means of regenerating the binary pulse train.

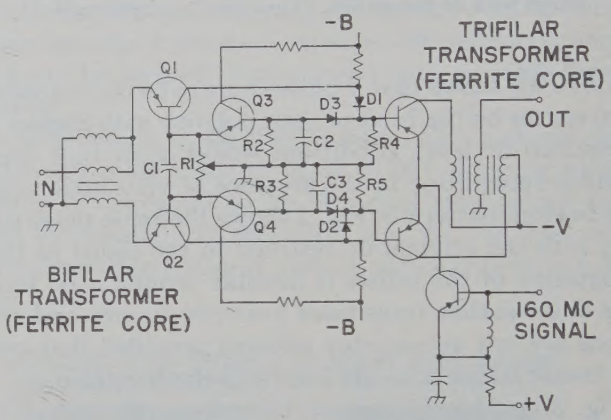

Fig. 7—DC restorer and gate.

Method 2—Code Translation for AC Recognition

Dicode[3] *Generator*

An alternate method of regenerating the pulses can be accomplished by means of changing the character of the pulse train to some code that has more desirable properties and then reconstructing it back into the original code. As was shown in Fig. 2, the change from one to zero or zero to one is always apparent even if the dc level of the signal is not transmitted. A circuit can be inserted in the transmission path preceding the regenerator that can recognize the changes from a one to zero or zero to one in the pulse train. The circuit that recognizes the change from ones to zeros or vice versa is called a dicode generator and is shown schematically, as constructed of 50-ohm cable, in Fig. 8.

The circuit functions as a subtraction network subtracting the energy of a time slot from the following time slot. By this method, a one preceded by a one or a zero preceded by a zero will result in no output. A one preceded by a zero will result in a positive pulse out and a zero preceded by a one will result in a negative pulse out. The input-output photographs of pulse trains show that information is obtained from the dicode generator only when the pulse train goes from one to zero or zero to one.

The output of the dicode generator has a constant (zero) dc level for any pulse pattern into it and so can steer a circuit unhampered by the low-frequency transmission characteristics preceding it with regard to different pulse patterns. Also, whereas the dc restorer indicated before depends upon a one or zero breaking up a string of zeros or ones within a certain time in order to maintain its operation, the dicode signal needs no such restriction.

The problem, however, is to reconstruct the binary signal from the dicode signal. This can be solved if we use the latter to steer a bistable circuit on and off.

High-Speed Code Translator

The circuit of a transistorized flip-flop (or dicode to binary translator), capable of cycling from one bistable state to the other and back in less than 6 mμsec, is shown in Fig. 9.

[3] The dicode principle is attributed to L. A. Meacham and is described by E. D. Sunde, "Theoretical fundamentals of pulse transmission," *Bell Sys. Tech. J.*, vol. 33, pp. 721–788; May, 1954.

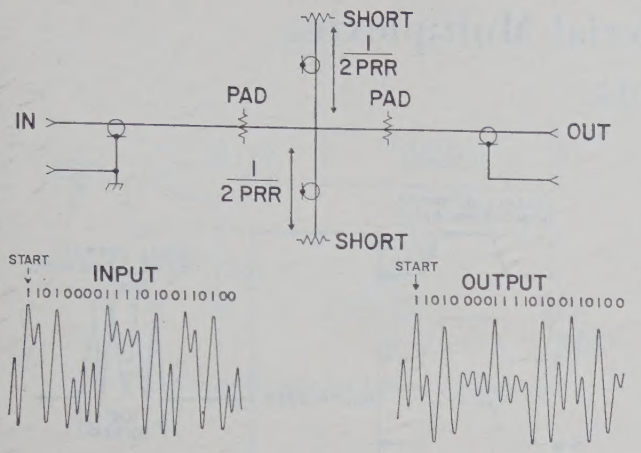

Fig. 8—Coaxial dicode generator.

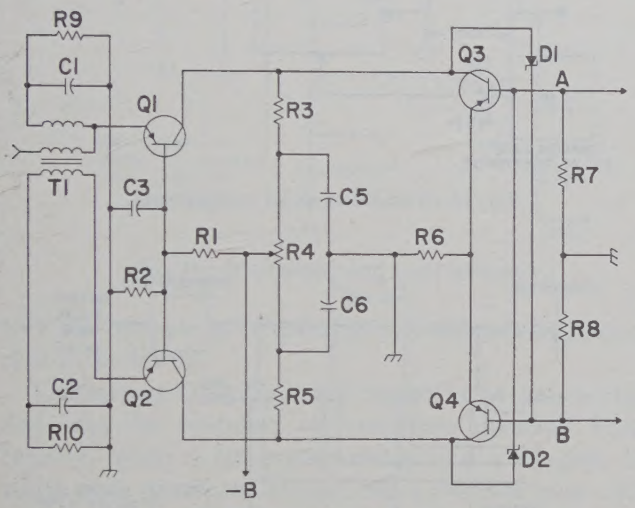

Fig. 9—High-speed code translator.

The dicode signal is applied balanced to the emitters of Q_1 and Q_2 which serve as buffer amplifiers to the flip-flop transistors Q_3 and Q_4. The signals of the collectors of Q_1 and Q_2 are applied to the bases of Q_4 and Q_3, respectively, through the conducting voltage reference diodes D_1 and D_2 which also serve as the cross-coupling for the flip-flop. A positive signal on one base is aided by a negative signal on the opposite base. This gives a double acting steering signal that helps speed the transition from one state to the other. The common emitter resistor insures that when one transistor is conducting, the other is cut off and also aids the transition as a common coupling element. Fig. 10 shows the input dicode signal to the translator and the boxcar binary output signal taken from the bases of Q_3 and Q_4.

The output of the translator is direct-coupled to the regenerative timing gate (previously described) to inject timing and to further regenerate the pulse train (Fig. 11).

Conclusion

Fig. 12 shows the input and output pulse forms for the two methods of pulse regeneration described in this paper. These waveforms are as presented on a sampling oscilloscope. They represent pulse code modulation signals at a bit rate of 160-mc in a 6.25-mμsec time slot. The input signal is shown as a band-limited signal with appreciable intersymbol interference. The dicode signal could be derived from this signal or else it could be transmitted over the transmission system. The output signal is common to both methods and is a signal in which spaces and pulses have both been retimed and regenerated. This type signal can be rectified in the timing channel of a repeater to provide relatively constant timing information regardless of the number of pulses or spaces received in a row.

Both of these regenerators were assembled on printed circuit cards and operated, with no apparent degradation from the performance observed, using conventional high-frequency point-to-point construction.

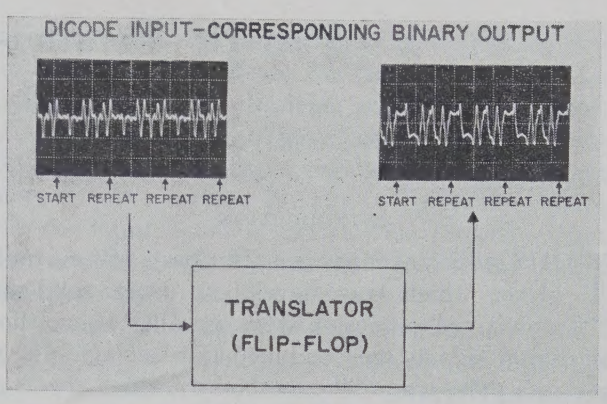

Fig. 10—Input-output signals of flip-flop.

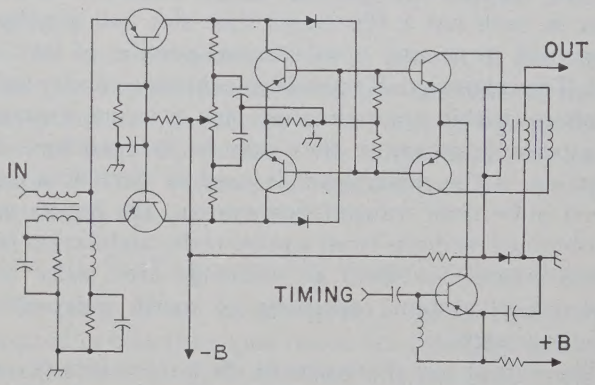

Fig. 11—Translator and gate.

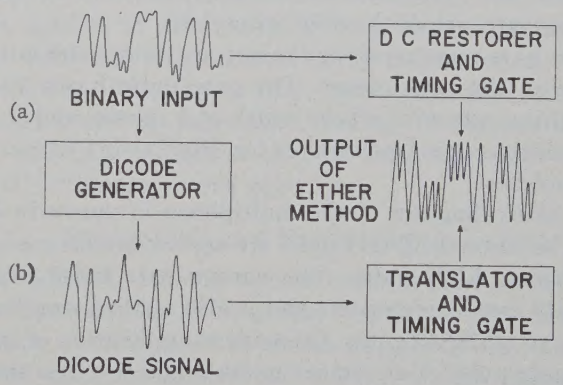

Fig. 12—Representative signals for two methods of pulse regeneration at a 160-mc bit rate.

Part II: Parallel-to-Serial Multiplexing

J. C. NOLL

Introduction

THIS section of the paper describes a 160-mc multiplexer which was developed using solid-state circuit techniques. Sixteen parallel 10-mc clock rate digital signals are combined into a single 160-mc clock rate pulse train. The method by which this is accomplished is shown in Fig. 13. Each of the sixteen parallel inputs is a digital signal with a 10-mc clock rate; that is, each has a 100-mμsec time slot and a pulse is presumed to occupy a substantial portion of its time slot. The input signals must be synchronous and roughly in phase (within approximately plus or minus a quarter of a period); otherwise they may be independent. For example, if the multiplexer is used as part of a high-speed pulse code transmission system, the inputs may be obtained as digits from a pulse code modulation television encoder or from an exchange area pulse code modulation system consisting of many independent telephone signals.

The output signal consists of the sixteen inputs compressed and combined into a 100-mμsec time slot. Thus, the time slot for each of the output pulses is 6.25-mμsec or one-sixteenth of the original period.

The gate pulse controls the output timing and output shape of the multiplexer. The gate pulse has a 10-mc repetition rate with a base width of 6 mμsec, and is obtained from a common source for distribution within the multiplexer.

A block diagram of the multiplexer is shown in Fig. 14. The sixteen digital inputs are applied simultaneously to sixteen AND gates. The narrow gate pulse is split equally into sixteen parts and is also applied simultaneously to all AND gates. Coincident application of input and gate pulse at all sixteen gates would result in simultaneous launching of six mμsec pulses at sixteen equally separated points on a broad-band delay line. The pulse from gate 1 will go into the regenerator almost immediately, but the pulse from gate 2 must travel through a 6.25-mμsec section of delay line and will arrive one time slot later. Thus, the space separation of the input is converted to time separation of the output.

Half of each pulse will travel in the opposite direction and in so traveling will be partially reflected at every gate location. The resulting interference can be kept within limits by appropriate circuit design and the residual interference can be further suppressed by a regenerator.

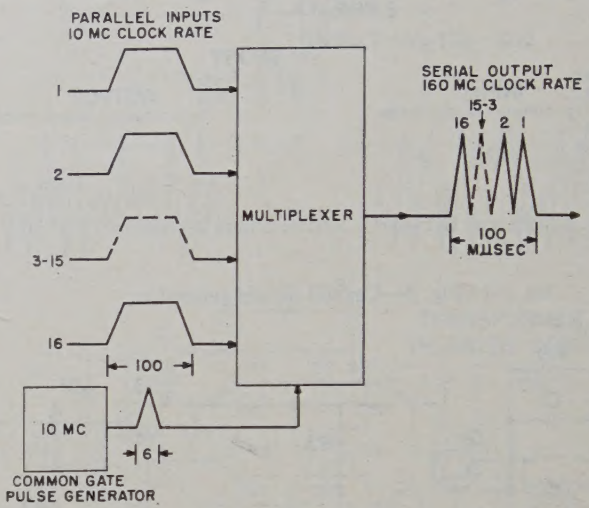

Fig. 13—Parallel-to-serial multiplexing.

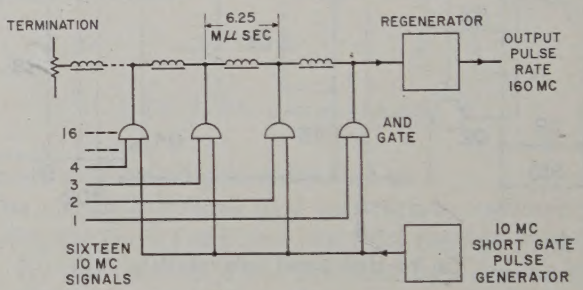

Fig. 14—Block diagram of 160-mc multiplexer.

Current Mode and Gate

A three-transistor current mode switching AND gate is used to launch pulses onto the line (Fig. 15). Transistors Q_1 and Q_2 are normally biased on and Q_3 is biased off. Q_1 and Q_2 act as sinks for the current source R_1. For the values shown, this current source would be about 18 ma. If either transistor is switched off by application of a base signal, the other transistor will take the entire current from R_1. When a 100-mμsec signal is applied to switch off Q_1 and the 6-mμsec gate pulse is applied to switch off Q_2, the current is diverted through Q_3 for the duration of the narrow gate pulse. If Q_1 and Q_2 are switched completely, then the entire current from R_1 appears at the output, independent of the amplitude of the input signal. The output wave shape and timing are largely determined by the gate pulse and are relatively insensitive to moderate variations of input signal level. Thus, the output pulses may be considered partially regenerated and timed.

Diffused-base (mesa) germanium transistors similar to 2N509 type are used in the AND gate. These particular transistors are specified for transmission use rather than for switching use and have grounded-base cutoff frequencies above 600 mc. A switching version of the 2N509, the 2N559, did not work as well principally because of its larger collector capacitance. 2N501 transis-

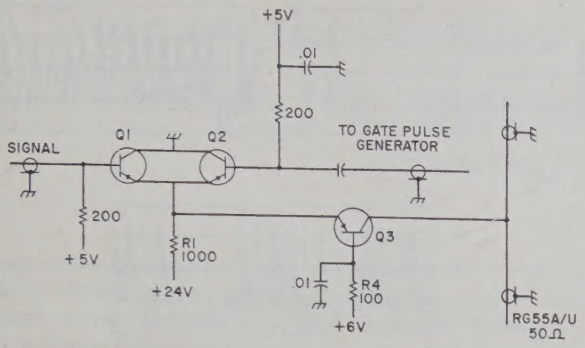

Fig. 15—AND gate for 160-mc multiplexer.

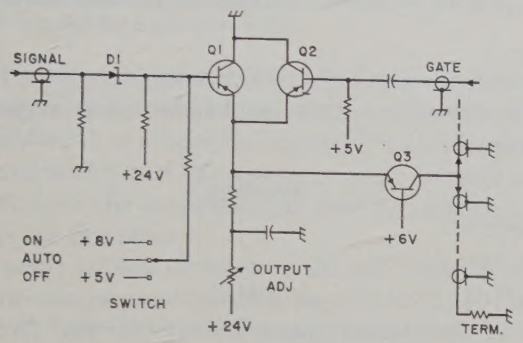

Fig. 16—Multiplexer and word generator.

tors will operate satisfactorily, but at lower emitter current drive levels.

Transistors Q_1 and Q_2 are biased in an active region and may be switched off (emitters reversed biased) rapidly. With a 100-mμsec signal and a 6-mμsec base width gate pulse, the output has a 6-mμsec base width; with a 4-mμsec base width input pulse (and 6-mμsec gate pulse properly phased), the output base width is 4-mμsec. We consider current-mode switching to be a salient feature of high-speed solid-state switching technique.[4,5]

The 2N509 requires from 0.3 to 0.6 volts forward base-emitter bias to obtain a collector current of 10 ma in the circuit of Fig. 15. However, the power required of the input pulses is determined by the input cable terminating resistors. That is, the current of the signal pulse must be such that the IR drop in the base resistors of Q_1 and Q_2 is equal to 0.3 to 0.6 volt mentioned above. For the bias values shown in Fig. 15, there is a threshold margin against noise; for a signal of +5.0 to +6.0 volts, there will be no output; for +6.5 to +7.0, the output will be relatively independent of the input. The margin will be determined by the allowed emitter-base breakdown voltage (1 to 2 volts) and the magnitude of signal available.

The signal input is direct-coupled to the output, which avoids the problem of dc restoration. However, it does have the disadvantage of requiring a different dc level for the input and output. To avoid this problem and to permit using the multiplexer as a word generator, the modifications of Fig. 16 have been incorporated into the AND gate. The voltage reference diode D_1 is biased so as to remain always in the avalanche breakdown region. For the input signal, it acts as a low impedance battery to translate the dc level of the signal to the dc level of the base of Q_1.

For the values shown in Fig. 15, an 18-ma peak pulse is obtained for an output voltage of 0.45 volts (18 ma into 25 ohms or 9 ma into 50 ohms). The maximum recommended steady emitter current is 20 ma for the 2N509 transistor, thus limiting the output level obtainable.

The variable resistor in series with R_1 is used to adjust the current available to the transistors, thereby adjusting the amplitudes of the output signals to any desired level. Particularly the amplitudes may be adjusted for the variation of loss suffered by the signals traversing the output delay line.

160-MC Bit Rate—10-MC Word Rate Generator

In place of an input signal, a dc voltage may be applied to bias the signal transistor Q_1. If, by means of a manual switch, Q_1 is switched off, the gate pulse will cause a 6-mμsec pulse to be launched every 100 mμsec. If Q_1 is biased on, there will be no output. If dc voltages are applied to all sixteen AND gates, an arbitrary 16-bit word will be generated every 100 mμsec. A 160-mc bit rate, 10-mc word rate, pulse generator has been found useful for laboratory testing. The inputs may be dc and/or ac signals so that the output word is a static and/or dynamic word generator.

Delay Line and Reduction of Echoes

RG55A/U 50-ohm coaxial cable is used as the delay line between the AND gates. With a velocity of propagation of 0.695 relative to free air, about 4.3 feet of coaxial cable is required for a delay of 6.25 mμsec. The cable delay line is also relatively broad-band, inexpensive, and low-loss. The pulse from the last gate must traverse fifteen more sections of delay line than the first, and is attenuated by about 2.5 db relative to the level of the first gate output. The levels are adjusted and made equal by means of the variable resistor mentioned earlier.

When the pulse travels toward the termination, it reflects from the impedance discontinuities caused by the transistor gate bridged across the line. When the pulse from one gate arrives at the location of another gate, the latter gate is in a nonconducting state and therefore the principle discontinuity is caused by the collector capacitance. This capacitance, which includes header and wiring capacitance, is of the order of three picofarads (pico $= 10^{-12}$). The discontinuity can be reduced by incorporating the capacitance as part of a low-pass constant-k filter. Removing the cable shield for a fraction

[4] R. K. Richards, "Digital Computer Components and Circuits," D. Van Nostrand Co., Inc., New York, N. Y., pp. 178–184; 1957.

[5] H. S. Yourke, "Millimicrosecond Transistor Current Switching Circuits," paper presented at IRE-AIEE Transistor and Solid-State Circuits Conf., University of Pennsylvania, Philadelphia; February 14–15, 1957; IRE Trans. on Circuit Theory, vol. CT-4, pp. 236–240; September, 1957.

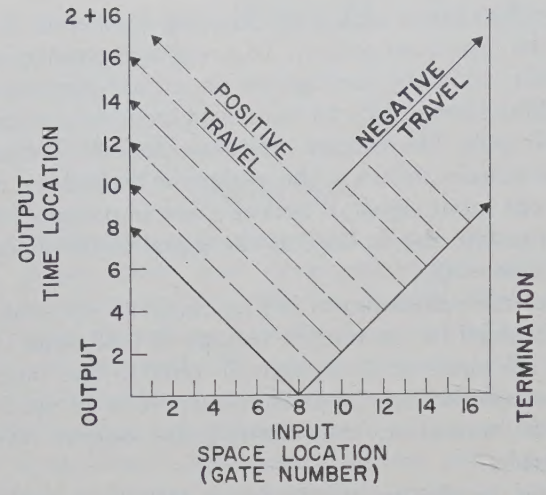

Fig. 17—Space-time plane indicating echoes.

of an inch on either side of the gate furnishes the inductance to form a filter with a cutoff frequency greater than 1000 mc.

To adjust the filter, a pulse is sent down the line and the magnitude of the reflected pulse is observed. A pulse hybrid transformer[2] is useful in separating the incident and reflected pulses and permits measuring return losses as low as 40 db. A 30-db return loss may be obtained by individually adjusting each filter and a 26-db return loss is obtained if transistors for Q_3 are randomly selected. As shown in Fig. 17, a given time slot may be contaminated by as many as eight primary pulse reflections. For this maximum of eight echoes, it is necessary to keep the return loss of each reflection to 30 db for an output signal-to-interference ratio of 12 db. A signal with a 12-db return loss may be successfully regenerated by use of the circuits and techniques described in Part I.

The hybrid technique used in conjunction with a Goodall stroboscope also permits adjusting the length of each line to 6.25 mμsec within an accuracy of ±0.1 mμsec. The stroboscope has a usable equivalent sweep speed to 10 cm/mμsec or a speed one-third that of light.

Gate Pulse

The gate pulse is obtained from a vacuum tube pulse generator. When high-frequency high-power transistors become more readily available, it is intended that this gate pulse will be generated by transistor circuits.

Performance

The photographs of Fig. 18 show the output of the multiplexer used as a static word generator without regeneration. The top trace shows a single pulse followed by fifteen spaces. The middle trace shows one pulse space followed by fifteen pulses, while the bottom trace shows an arbitrary word. The bit rate is 160 mc (6.25-mμsec time slot) with a word repetition rate of 10 mc. Fig. 18(a) and (b) show especially the effects of pulse reflections in the output line. It is evident that a clear distinction may be made between pulses and spaces.

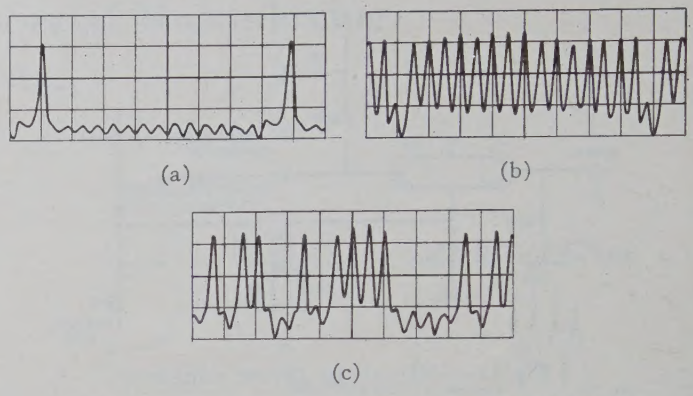

Fig. 18—Output of multiplexer before regeneration.

However, to reduce the unwanted signal on the base line and to make the output amplitudes equal, regeneration is required.

Appendix

Components

The Western Electric transistors used in these circuits are A2104 (2N509)-type diffused-base germanium units. Some of the typical characteristics for the 2N509 are:

h_{fb}	(I_E=10 ma, V_{CB}=−10 vdc, f=1 kc)	0.98
h_{fe}	(I_E=10 ma, V_{CB}=−10 vdc, f=100 mc)	15.5 db
f_{ab}	(I_E=10 ma, V_{CB}=−10 vdc)	750 mc
h_{rb}	(I_E=10 ma, V_{CB}=−10 vdc)	$1 \cdot 3 \cdot 10^{-3}$
r_b'	(I_E=10 ma, V_{CB}=−10 vdc, f=250 mc)	100 ohms
I_{CO}	(I_E=0, V_{CB}=−20 vdc)	2 μa
C_C	(I_E=0, V_{CB}=−10 vdc)	2.5 pf
P	(maximum continuous)	150 mw.

The high-speed translator required that transistors be selected to achieve the highest speeds; however, in all other circuits nonselected transistors operated satisfactorily.

The high-speed silicon diodes used in the dc restorer circuit are Bell Laboratories M-2111 computer diodes. These diodes have a capacity of about 1.0 pf (at zero volts).

The voltage reference diodes used as direct coupling devices are Western Electric 420-type silicon alloy junction diodes. They are similar to quarter-watt voltage reference diodes manufactured by many diode suppliers. In the circuits shown, they are always biased in the avalanche conduction region.

Acknowledgment

The authors gratefully acknowledge the assistance of many colleagues at Bell Telephone Laboratories. They are particularly indebted to M. E. Hines for his assistance and to W. M. Goodall, O. E. DeLange, and C. L. Ruthroff of the Holmdel Bell Telephone Laboratories for their pioneering research in high-speed pulse generation, transmission, and measuring techniques.

A Note on the Number of Internal Variable Assignments for Sequential Switching Circuits*

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Summary—**An important step in the synthesis of sequential switching circuits is the assignment of binary variable states to represent internal states of the circuit. A formula is derived here which indicates the number of different assignments which can be made for flow tables having a given number of rows. There are only three essentially different assignments possible for a four-row table, and there are 140 for a five-row table.**

THE terminal characteristics of sequential switching circuits can be specified by means of flow tables,[1–3] as shown in Table I. The columns represent input states and the rows represent internal states. The entries in the table indicate the next internal state. Outputs are not shown.

TABLE I
A FLOW TABLE AND FOUR ROW ASSIGNMENTS

	Input x_1x_2				y-states y_1y_2			
State	00	01	11	10	(a)	(b)	(c)	(d)
1	1	1	1	2	00	00	00	10
2	1	2	2	3	01	11	01	00
3	1	3	2	4	10	10	11	01
4	1	4	3	1	11	01	10	11

A general synthesis procedure can be carried out as follows:

1) Construction and simplification of the flow table.[2]
2) Assignment to each row of the table of a unique state of a set of binary valued variables which will be called "state variables."
3) Derivation from the flow table and row assignment of the specifications for a combinational circuit with feedback.[2]
4) Synthesis of this combinational circuit by any convenient method.[3]

This paper will be concerned with step 2). Consider the case of an r-row flow table. (For the present we restrict the discussion to synchronous functions.) In order to provide r distinct states, at least $\log_2 r$ state variables are necessary. Let s be the smallest integer meeting this condition for a given r. We will then have available 2^s states to assign to the r-rows. The number of possible assignments is thus $(2^s)!/(2^s-r)!$. However, from a physical point of view, many of these assignments are essentially equivalent to one another, since they differ only in that some of the state variables have merely been relabelled. For example, the assignment labelled (d) in Table I can be obtained from the one labelled (c) by complementing y_2 and then interchanging y_1 and y_2.

We shall demonstrate that the number of distinct row assignments for an r-row flow table is

$$N = \frac{(2^s - 1)!}{(2^s - r)!s!} \cdot$$

(This result in less general form was derived by Unger.[4]) The values of N for $r = 1, 2, \cdots, 9$ are indicated in Table II. Note the sharp increases that occur following values of r which are powers of 2. This effect occurs because s increases at these points. The result is that for tables with less than five rows it is not at all difficult to try all of the different row assignments with the idea of finding the "best" circuit. For r between 5 and 8, a group effort would be required to handle the job. When r exceeds 9, the ability of even a modern computer would be taxed.

TABLE II

Number of Rows	s	Number of Assignments
1	0	1
2	1	1
3	2	3
4	2	3
5	3	140
6	3	420
7	3	840
8	3	840
9	4	10,810,800

It would obviously be desirable to have a method for ascertaining *a priori* which assignment is the best one according to some criterion such as the minimization of the resulting circuit. Unfortunately, this seems to be an exceedingly difficult problem and we can offer no suggestions as to how it can be approached.

In Table I we have shown three distinct assignments labelled (a)–(c) for the four-row flow table. The first as-

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‡ Bell Telephone Labs., Whippany, N. J.

[1] E. F. Moore, "Gedanken experiments on sequential machines," in "Automata Studies," Princeton University Press, Princeton, N. J.; 1956.

[2] D. A. Huffman, "The synthesis of sequential switching circuits," *J. Franklin Inst.*, vol. 257, pp. 161–190, 275–303; March/April, 1954.

[3] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y.; 1958.

[4] S. H. Unger, "Row Assignments in Sequential Switching Circuits," Res. Lab. of Electronics, Mass. Inst. Tech., Cambridge, Quart. Progress Rept.; June, 1956.

signment was selected at random. The second assignment was obtained from the first by interchanging the states assigned to rows 2 and 4. Interchanging rows 3 and 4 of the (a) assignment produced the arrangement designated as (c).

It should be noted that for some functions the number of row assignments leading to physically different circuits may be less than our formula indicates due to symmetries in the flow table. In the case of asynchronous functions it is necessary to restrict our attention to those assignments that do not lead to critical race conditions.[2] These will constitute a subset of the class we have counted.

Derivation of Formula

There are 2^s states of s binary variables and the number of different ways of assigning these states to r rows of a flow table is $(2^s)!/(2^s-r)!$. There are $s!$ permutations of these binary variables, 2^s ways of complementing binary variables, and thus $s!2^s$ ways of permuting and complementing the s binary variables. One method for generating all assignments would be to pick one particular assignment, A_0, and then to apply all $s!2^s$ combinations of permutations and complementations to generate other assignments: G_0A_0, G_1A_0, $\cdots$, $G_{s!2^s}A_0$ where the G_i represent the various permuting and complementing operations and G_iA_0 represents the assignment which results from applying the G_i operation to assignment A_0. Another assignment A_1 which is not equal to A_0 or to any G_iA_0 is then selected, and the G_i operations are carried out to obtain G_1A_1, G_2A_1, etc. An assignment A_2 not equal to any previously generated assignment is then chosen and the process is repeated until all $2^s!/(2^s-r)!$ different assignments have been exhausted. The A_i's will be shown to constitute a set of distinctly different assignments, that is, assignments which may lead to different circuits.

Theorem: Each of the G_iA_h obtained in this procedure will be distinct; *i.e.*, there will be no G_i, A_h, G_j, and A_k for which $G_iA_h=G_jA_k$ unless $i=j$ and $h=k$.

Proof: It has been shown by Shannon[5] that the operations G_i form a group. Thus for every G_i there must exist an inverse operation G_i^{-1} such that $G_iG_i^{-1}=G_i^{-1}G_i=G_0$ where G_0 is the identity operation (for every h, $G_0A_h=A_h$).

Case 1—$G_iA_h=G_iA_k (i=j,\ h\neq k)$. Then $G_i^{-1}G_iA_h=G_i^{-1}G_iA_k$, which leads to $G_0A_h=G_0A_k$, and hence $A_h=A_k$, contradicting the assumptions.

Case 2—$G_iA_h=G_jA_k (i\neq j,\ h\neq k)$. Assuming $h>k$ we multiply both sides by G_i^{-1} to obtain

$$G_i^{-1}G_iA_h=G_i^{-1}G_jA_k,\ A_h=G_i^{-1}G_jA_k;$$

letting $G^*=G_i^{-1}G_j$ this becomes $A_h=G^*A_k$. But this contradicts the assumptions made in choosing the A_i's, namely, that if $i>j$ then $A_i\neq G_kA_j$ for any k.

Case 3—$G_iA_h=G_jA_h (i\neq j,\ h=k)$. This is equivalent to $A_h=G_i^{-1}G_jA_h$ where $G_i^{-1}G_j$ does not equal G_0 since $i\neq j$. The only way for this to be possible is if A_h has some columns which are identical or which are complementary.[6] However, A_h can not have such columns and still require only s variables to distinguish r rows. Removing one of a pair of identical or complementary columns does not change the number of rows which are distinguished.

Since 1) each of the G_iA_h are distinct, 2) there are a total of $2^s!/(2^s-r)!$ such assignments, and 3) there are $s!2^s$ assignments corresponding to each A_i, then there must be $N=2^s!/s!2^s(2^s-r)!=(2^s-1)!/s!(2^s-r)!$ of the A_i's.

If more than s state variables are used,[7] this formula is unsatisfactory since some of the assignments counted are degenerate; *i.e.*, they have some state-variable constant for all rows, or have two or more identical state variables.[8]

For certain special cases the following formulas have been obtained (v equals the number of state variables). Let $C(r)=2^{r-1}-1$. Then if $v=C(r-1)$,

$$N=\binom{C(r)}{C(r-1)}-\binom{r}{2}.$$

If $v>C(r-1)$ then

$$N=\binom{C(r)}{v}.$$

Some representative values are shown in Table III.

TABLE III

Number of Rows	v	Number of Assignments
4	3	29
5	4	1015
5	5	2793

[5] C. E. Shannon, "The synthesis of two-terminal switching circuits," *Bell Sys. Tech. J.*, vol. 28, pp. 59–98; January, 1949.

[6] E. J. McCluskey, Jr., "Detection of group invariance or total symmetry of a Boolean function," *Bell Sys. Tech. J.*, vol. 35, pp. 1445–1453; November, 1956.

[7] It is not clear that a minimal-cost sequential circuit is always obtained by using the minimum number of state variables; therefore, it would be reasonable to consider using more than s state variables. It is even more likely that more than s state variables would be used in the case of iterative networks, since there is no need for amplification to be provided for each state variable, and many relay iterative networks cannot be realized using only s state variables. E. J. McCluskey, Jr., "Iterative combinational switching networks—general design considerations," IRE Trans. on Electronic Computers, vol. EC-7, pp. 285–291; December, 1958.

[8] The following formula for the number of nondegenerate different assignments using v variables has been obtained by E. N. Gilbert of Bell Telephone Laboratories, Whippany, N. J.:

$$N=\frac{r!}{v!}\sum_{j=1}^{v}S(v+1,j+1)2^{-j}\binom{2^j}{r}$$

where the $S(n,k)$ are Stirling numbers of the first kind.

Synthesis of Minimal-State Machines*

SEYMOUR GINSBURG†

Summary—A technique is presented which yields a minimal-state machine satisfying a given set of behavioral specifications. The machine is constructed in the same manner as has commonly been done in the past in synthesizing a "primitive flow table." This contribution consists, not in describing a new method of synthesizing machines, but in showing that a particular instance of an established method yields a minimal-state machine. It is shown that the basic synthesis technique may be slightly modified so as to be applicable to obtaining a minimal-state machine which has the stability conditions desired when working with unclocked circuits.

I. Introduction

A CENTRAL problem in sequential switching theory is that of synthesis. In general, synthesis consists of trying to find a "system" that satisfies a prescribed set of requirements. For switching circuits the synthesis problem consists of finding a switching circuit that satisfies a given set of switching requirements.

Prior to 1954 there was a wide variety of methods available to the designer of sequential switching circuits [7], each method useful in certain situations. However, there was no single practical method which was applicable to most cases. In 1954 Huffman introduced such a procedure for synthesizing circuits from a prescribed set of *behavioral* requirements, the so-called *flow table* and *secondary assignment* methods [6].

Once the problem of finding one sequential switching circuit satisfying certain behavioral requirements was solved, new problems were open for consideration. Foremost among these were:

1) To find a switching circuit satisfying the synthesis requirements in which the amount of logic is minimum (in some sense) among all circuits satisfying the requirement.
2) To find a switching circuit satisfying the synthesis requirements in which the number of storage components (such as relays and flip-flops) is minimum among all circuits satisfy the requirements.

In what follows, attention is confined to the second problem exclusively, that is, to minimization of the storage components. With respect to this problem it is convenient to introduce the model of a switching circuit devised by Moore [9] and Mealy [8] called a *machine*. A known technique, the secondary assignment procedure, always yields a (clocked) switching circuit from a given machine [6], [1]. In general, the fewer the states in the machine, the fewer the number of storage components in the associated switching circuit. For this reason, as regards the synthesis of minimal storage component (clocked) switching circuits, it is possible to confine the discussion to the synthesis of minimal-state machines. This is done in the rest of the paper since, among all models for sequential switching circuits, the one which has proven most adaptable to precise mathematical analysis is the machine.

Now suppose a specific set of synthesis requirements (in the form of behavioral conditions) is given. Consider the problem of obtaining a minimal-state machine satisfying these requirements.

a) If the requirements are of a very special character, it may be possible, by direct means, to obtain a minimal-state machine satisfying the requirements. (Naturally the method will depend on the nature of the requirements.[1])

b) When the requirements are not of a very special nature, there is no known method for obtaining a minimal-state machine satisfying the requirements. The following process is then executed:

3) Find a machine T satisfying the prescribed requirements. This is accomplished by the flow table procedure of Huffman, applied to machines.
4) Find a minimal-state machine R_T which can do everything that T can do (from the input-output point of view) [5], [10].

The machine R_T obtained in 4) automatically satisfies the synthesis requirements since, behaviorally speaking, R_T can do everything that T can do; and the behavior of T satisfies the specifications. In designing switching circuits it has been customary to use R_T as an approximation to a minimal-state machine satisfying the synthesis requirements. In general, R_T is *not* a minimal-state machine satisfying the synthesis requirements. This is because the machine T obtained in 3), and thus R_T, usually has many behavioral conditions inherent in it which are not in the original specifications. In fact, if T_1 and T_2 are two distinct machines satisfying the synthesis requirements, and if R_{T_1} and R_{T_2} are the machines obtained from 4), it frequently happens that the number of states in R_{T_1} is not equal to the number of states in

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[1] This is so, for example, in case the requirements are in the form of a finite set of finite sequences of inputs vs finite sequences of outputs [3]. By oral communication the author has been informed that R. E. Miller has treated the situation where the synthesis conditions are explicitly in the form of a finite number of input-output sequences, each either of finite length or ultimately periodic.

R_{T_2}. Thus steps 3) and 4) form a suboptimization procedure in the sense that it is a procedure yielding a machine which is minimal among all machines satisfying all input-output conditions inherent in T, but not necessarily minimal with respect to the original specifications.

There are two main results to this paper. The first is a technique which, depending on a given set of behavioral specifications, yields a minimal-state machine satisfying the specifications (Section IV), and is thus an instance of a). However it uses the procedure of b) in that it involves constructing, in a special way, a machine S satisfying the requirements and then reducing S as much as possible. The machine S is constructed in the same manner as has commonly been done in the past in synthesizing a "primitive flow table." The contribution here thus consists, not in describing a new method of synthesizing machines, but in showing that a particular instance of an established method yields a minimal state machine.

The second main result is to show that the basic synthesis technique may be slightly modified so as to be applicable in obtaining a minimal-state machine (with respect to a suitable set of specifications) which has the stability conditions desired when working with unclocked circuits (Section V). The modification essentially consists of adding one step (Theorem 1) after the reduction procedure [*i.e.*, step 4]. The purpose of this extra step is to guarantee that the resulting machine is one having the desired stability conditions.

II. Basic Terms

By a (deterministic) sequential machine S, abbreviated by *machine* S, is meant a finite number of inputs $I^1, \cdots, I^m$; a finite number of (internal) states $q_1, \cdots, q_n$; a finite number of outputs $E^1, \cdots, E^r$; and two functions δ_S and λ_S, written δ and λ for short when S is understood. For some (possibly all) pairs (q, I), q a state and I an input, δ takes (q, I) into a state $\delta(q, I)$, and for some (possibly all) pairs (q, I), λ takes (q, I) into an output $\lambda(q, I)$. Given the inputs, the outputs, and the states, a machine is thus determined when δ and λ are specified for certain (q, I). A machine is usually given in matrix form as shown in Fig. 1. [Some of the rectangles have a δ or a λ (or both) entry.] A matrix as given in Fig. 1 is called a δ, λ matrix.

Let $I_1, \cdots, I_k$ be a sequence of inputs to a machine S and let p_1 be a state of S. $\lambda(p_1, I_1, \cdots, I_k)$ is said to exist if each output $\lambda(p_1, I_1), \cdots, \lambda(p_k, I_k)$, and each state $p_{i+1}=\delta(p_i, I_i)$ for $i<k$ exist; and $\lambda(p_1, I_1, \cdots, I_k)$, when it exists, is defined to be $\lambda(p_1, I_1)\lambda(p_2, I_2) \cdots \lambda(p_k, I_k)$. $\delta(p_1, I_1, \cdots, I_k)$ is said to exist if each state $p_{i+1}=\delta(p_i, I_i)$ for $i \leqq k$ exists; and $\delta(p_1, I_1 \cdots I_k)$, when it exists, is defined to be the state p_{k+1}. Thus $\lambda(p_1, I_1, \cdots, I_k)$ is the output obtained when the sequence of inputs $I_1, \cdots, I_k$ is applied to the machine initially in state p_1; and $\delta(p_1, I_1, \cdots, I_k)$ is the state the machine goes to from state p_1 upon insertion of the sequence of inputs $I_1, \cdots, I_k$.

	I^1	$\cdots$	I^i	$\cdots$	I^m
q_1	$\delta(q_1, I^1)$				
$\vdots$					
q_j			$\delta(q_j, I^i)\lambda(q_j, I^i)$		
$\vdots$					
q_n					$\lambda(q_n, I^m)$

Fig. 1—δ, λ matrix.

Observe that

$$\lambda(p_1, I_1, \cdots, I_k) = \lambda(p_1, I_1, \cdots, I_j)\lambda(\delta(p_1, I_1, \cdots, I_j), I_{j+1}, \cdots, I_k)$$

whenever either side exists, and

$$\delta(p_1, I_1, \cdots, I_k) = \delta(\delta(p_1, I_1, \cdots, I_j), I_{j+1}, \cdots, I_k)$$

whenever either side exists.

A sequence of inputs $I_1, \cdots, I_k$ is said to be *applicable* to a state p_1 if $\lambda(p_1, I_1, \cdots, I_k)$ exists.

Notation

Let S and T be two machines. For states p in S and q in T, by $p \leqq q$ is meant that each sequence $I_1, \cdots, I_k$ of inputs which is applicable to p is applicable to q, and, in addition, $\lambda_S(p, I_1, \cdots, I_k)=\lambda_T(q, I_1, \cdots, I_k)$. Given two machines S and T, by $S \leqq T$ is meant that to each state p in S there exists a state $f(p)$ in T satisfying $p \leqq f(p)$.

Roughly speaking, for states p in S and q in T, $p \leqq q$ means that everything that S can do starting at p, machine T can do starting at q. $S \leqq T$ means that machine T can do everything that machine S can do.

In [4] the following problem was introduced:

Problem Q: Given a machine T, find a machine W satisfying the following two properties:

1) $T \leqq W$.
2) The number of states in W is not greater than the number of states in any other machine Y for which $T \leqq Y$ holds.

For a given machine T there now exist methods which yield solutions to Problem Q [5], [10]. It will be assumed in what follows that the reader is familiar with these methods.

III. Synthesis Conditions

As mentioned in the Introduction, one of the two principal results of this paper is to show that a particular case of an established method (the method of constructing a flow table) frequently yields a minimal-state machine. Thus the technique presented here is, at best, applicable only to those synthesis conditions capable of being satisfied by the more general method. The

author is not aware of any written work in which those synthesis conditions are explicitly (or even implicitly) described, that is, put into a formal language. Certainly it does not appear in the two foremost printed expositions of the flow table method [6], [1]. It is a fact that, using methods from symbolic logic, research on synthesis procedures has been done [2]. Also, work on a general language to describe the behavior of machines is currently being done at the University of Michigan and at the University of Pennsylvania. The ticklish problem of listing all mathematical forms of the synthesis conditions to which our technique has application will be avoided. Instead, it will be assumed that the synthesis conditions are in such a form as to be satisfied by a machine X *if and only if there exists a finite number of states in* X *having a specified input-output behavior, i.e.*, if and only if there exists a finite number of states q such that the application of certain input sequences (depending on q) to the machine initially at q yields certain output sequences. Practically all the problems appearing in [6] and [1] are of this form.

IV. The Synthesis Technique

Suppose that a set of synthesis conditions of the nature described in Section III is given. The synthesis technique will now be explained in two stages.

The first stage consists of constructing a machine S as follows. For each distinct input-output behavior demanded by the specifications, assign a state, designated by the symbol q, to yield exactly this input-output behavior. Denote by $A(q, I)$ the set of input-output sequences which result when the input I and the output $\lambda(q, I)$ are removed from the first position in the input-output sequences associated with q. Let $\delta(q, I)$ be a state which is assigned to yield the input-output behavior consisting of precisely the input-output sequences in $A(q, I)$. Clearly the machine S, consisting of all the states q together with the δ and λ functions, satisfies the prescribed input-output behavior, and thus the specifications.

The most important property that S possesses is that for any machine T, $S \leqq T$ *if and only if* T satisfies the specifications.[2] Suppose that $S \leqq T$. For each input-output behavior demanded by the synthesis conditions, there exists a state q in S satisfying it. Since $S \leqq T$, there exists a state p in T so that $q \leqq p$. Then p and, thus, T satisfy this input-output behavior. Therefore T contains a set of states which satisfy the specified input-output behavior. By the basic assumption about the synthesis conditions, T satisfies the synthesis conditions.

[2] For certain synthesis conditions of a more general nature than considered here, as, for example, conditions limiting *all* the outputs of the desired machine to be elements of a particular set, this statement must be generalized as follows: "The most important property that S possesses is that for any machine T, $S \leqq T$ if and only if T *contains a submachine* T^* which satisfies the specifications." [The machine T^* is said to be a submachine of T if each state, input, and output of T^* is a state, input, and output respectively of T. Furthermore, $\lambda_{T^*}(q, I) = \lambda_T(q, I)$ for each input I which is applicable to q in T^*, and $\delta_{T^*}(q, I) = \delta_T(q, I)$ whenever $\delta_{T^*}(q, I)$ exists.]

Now suppose that T is any machine satisfying the synthesis conditions. Let q be any state of S. From the way S is defined, the input-output behavior of q is exactly the input-output sequences demanded by the specifications for some state. Since T satisfies the specifications, there exists a state p in T which satisfies these input-output sequences (in addition to other input-output sequences). Hence $q \leqq p$. Thus $S \leqq T$.

The second stage of the synthesis procedure is to find a solution W to Problem Q for S. This may be done in any convenient way, such as that given in [5] and [10].

Since $S \leqq W$, W satisfies the synthesis conditions. Suppose that T is any machine satisfying the synthesis conditions. Then, as noted above, $S \leqq T$. Since W is a solution to Problem Q for S, the number of states in W is equal to or smaller than the number of states in T. It follows that W is a minimal-state machine satisfying the synthesis conditions.

In this section and the next, the synthesis procedure will be applied to problems involving different synthesis conditions. It is intended that the variety of examples presented be a representative sample, not a complete list, of the types of problems capable of being solved by the synthesis procedure.

First Application

Suppose that the synthesis conditions are stated explicitly in the form of a finite number of input-output sequences, each either of finite length or cyclically infinite.[1] Let the input-output sequences of finite length be

$$\begin{array}{ll} \text{input sequence} & I_1^i \cdots I_{n(i)}^i \\ \text{output sequence} & E_1^i \cdots E_{n(i)}^i \end{array} \qquad 1 \leqq i \leqq r;$$

and the cyclically infinite input-output sequences be

$$\begin{array}{ll} \text{input sequence} & I_1^i \cdots I_{k(i)}^i \overbrace{I_{k(i)+1}^i \cdots I_{n(i)}^i}^{\text{cyclic}} \\ \text{output sequence} & E_1^i \cdots E_{k(i)}^i \underbrace{E_{k(i)+1}^i \cdots E_{n(i)}^i}_{\text{cyclic}} \end{array} \qquad r+1 \leqq i \leqq s.$$

In accordance with the synthesis technique, associated states with the input-output behavior are as indicated below.

$$\begin{array}{l} I_1^i \cdots I_{n(i)}^i \\ q_1^i \cdots q_{n(i)}^i \\ E_1^i \cdots E_{n(i)}^i \end{array} \qquad 1 \leqq i \leqq s.$$

Define the λ and δ functions as follows. Let $\lambda(q_j^i, I_j^i) = E_j^i$ for $1 \leqq i \leqq s$ and $1 \leqq j \leqq n(i)$. Let $\delta(q_j^i, I_j^i) = q_{j+1}^i$ for $1 \leqq i \leqq s$ and $j < n(i)$; and for $r+1 \leqq i \leqq s$, let $\delta(q_{n^i(i)}^i, I_{n^i(i)}^i) = q_{k^i(i)+1}^i$. The states q_j^i together with the two functions δ and λ form the machine S. A machine W which is a solution

to Problem Q for S is a minimal-state machine satisfying the input-output sequences.

As a specific instance, suppose that the input-output sequences are

$$\begin{array}{ll} a\ b & a\ \overbrace{a\ b\ a}^{\text{cyclic}} \\ & \text{and} \\ 0\ 0 & 1\ \underbrace{0\ 1\ 0}_{\text{cyclic}}. \end{array}$$

The assignment of the states yields

$$\begin{array}{ll} a\ b & a\ \overbrace{a\ b\ a}^{\text{cyclic}} \\ q_1{}^1q_2{}^1 & q_1{}^2q_2{}^2q_3{}^2q_4{}^2 \\ 0\ 0 & 1\ \underbrace{0\ 1\ 0}_{\text{cyclic}} \end{array}$$

The δ, λ table for S is in Fig. 2. The δ, λ table for W, a solution to Problem Q for S, is in Fig. 3. In W $p_1=\{q_1{}^1,\ q_2{}^1,\ q_4{}^2\}$, $p_2=\{q_2{}^1,\ q_2{}^2\}$, and $p_3=\{q_1{}^2,\ q_3{}^2\}$.[3] The machine W is a minimal-state machine satisfying the original specifications.

Second Application

Let I_t denote the present input, E_t the present output, I_{t-i} the ith previous input, and E_{t-i} the ith previous output. In a large number of problems the synthesis specifications are expressed in the form[4]

$$E_t = f(I_{t-r}, \cdots, I_t, E_{t-s}, \cdots, E_{t-1}), \qquad (1)$$

together with some additional conditions. Two additional conditions which frequently occur are listed below.

Condition 1—The desired machine is to have a start state q_1 with the following property. There exist nonnegative integers r and s and certain sequences $\{I_j\}$ of inputs applicable to q_1 such that

a) for $t \leqq \max\{r, s\}$, the output E_t depends on the t inputs $I_1, \cdots, I_t$;

b) for $t < \max\{r, s\}$ and certain sequences $E_{t-s}, \cdots, E_{t-1}$ of outputs (depending on $I_{t-r}, \cdots, I_{t-1}$)

$$E_t = f(I_{t-r}, \cdots, I_t, E_{t-s}, \cdots, E_{t-1});$$

c) the sequences $\{I_j\}$ not covered in either a) or b) are don't-care input sequences.

It will now be shown that the synthesis technique may be successfully employed in those problems where the synthesis conditions are (1) and condition 1 above.

[3] It is known that for any solution W to Problem Q for a machine S, the states of W may be considered to be sets of states of S [10]. This fact will be tacitly used in what follows.

[4] A machine having property that $E_t=f(I_{t-r}, \cdots, I_t, E_{t-s}, \cdots, E_{t-1})$ for all sequences of inputs $I_{t-r}, \cdots, I_t$ of length $r+1$ and all sequences of outputs $E_{t-s}, \cdots, E_{t-1}$ of length is said to be I, E dependent of maximal extent r, s [11].

	a	b
$q_1{}^1$	$q_2{}^1$ 0	0
$q_2{}^1$		
$q_1{}^2$	$q_2{}^2$ 1	
$q_2{}^2$	$q_3{}^2$ 0	
$q_3{}^2$		$q_4{}^2$ 1
$q_4{}^2$	$q_2{}^2$ 0	

Fig. 2—Machine S.

	a	b
p_1	p_2 0	0
p_2	p_3 0	0
p_3	p_2 1	p_1 1

Fig. 3—Machine W.

In view of a) and b), if $t \leqq \max\{r, s\}$ then E_t depends on $I_{t-r}, \cdots, I_t$; and if $t > \max\{r, s\}$ then E_t depends on $I_{t-r}, \cdots, I_t, E_{t-s}, \cdots, E_{t-1}$ (thus ultimately on $I_1, \cdots, I_t$). Let q_1 be the start state. For $k < \max\{r, s\}$, associate a distinct state q with each applicable sequence $I_1, \cdots, I_k$. For $k \geqq \max\{r, s\}$, associate a distinct state q with each sequence $I_{k-r+1}, \cdots, I_k$, $E_{k-s+1}, \cdots, E_k$ having the property that $I_{k-r+1}, \cdots, I_k, I_{k+1}, E_{k-s+1}, \cdots, E_k$ is a sequence in b) for some input I_{k+1}. The synthesis technique may then be applied to construct δ and λ, then S, and finally W.

As an illustration of the preceding, consider the following example.

The inputs of interest are 00, 01, 10, 11, and the outputs are 0 and 1. The don't-care input sequences are all those input sequences in which at least one of the eight pairs of inputs next listed occur in the order given:

00, 00; 00, 11; 01, 01; 01, 10; 10, 10; 10, 01; 11, 11; 11, 00.

For the remaining input sequences, starting from q_1, an output of $E_t=1$ occurs if and only if $I_{t-2}=00$, $I_{t-1}=10$, $I_t=11$, or $I_{t-2}=00$, $I_{t-1}=01$, and $I_t=11$.

Clearly the output depends only on the present input and the two previous inputs. In accordance with the above procedure, where $r=2$ and $s=0$, associate q_2 with 00; q_3 with 00, 01; q_4 with 00, 10; q_5 with 10; q_6 with 10, 00; q_7 with 10, 11; q_8 with 01; q_9 with 01, 00; q_{10} with 01, 11; q_{11} with 11; q_{12} with 11, 01; and q_{13} with 11, 10. Then machine S is constructed as given in Fig. 4. Machine W is given in Fig. 5, where $p_1=\{q_1, q_5, q_7, q_8, q_{10}, q_{11}, q_{12}, q_{13}\}$ and $p_2=\{q_2, q_3, q_4, q_6, q_9\}$, p_1 being the start state. W is a minimal-state machine with respect to the original specifications.

As another illustration consider the following example.

	00	01	10	11
q_1	q_2 0	q_8 0	q_5 0	q_{11} 0
q_2		q_3 0	q_4 0	
q_3	q_9 0			q_{10} 1
q_4	q_6 0			q_7 1
q_5	q_6 0			q_7 0
q_6		q_3 0	q_4 0	
q_7		q_{12} 0	q_{13} 0	
q_8	q_9 0			q_{10} 0
q_9		q_3 0	q_4 0	
q_{10}		q_{12} 0	q_{13} 0	
q_{11}		q_{12} 0	q_{13} 0	
q_{12}	q_9 0			q_{10} 0
q_{13}	q_6 0			q_7 0

Fig. 4—Machine S.

	00	01	10	11
p_1	p_2 0	p_1 0	p_1 0	p_1 0
p_2	p_2 0	p_2 0	p_2 0	p_1 1

Fig. 5—Machine W.

Let the inputs of interest be 0 and 1, and the outputs 0 and 1. The output E_t is determined by the formula

$$E_t = I_t + E_{t-1} + E_{t-2} \pmod 2.$$

The only sequences of inputs of interest are those in which a zero follows a one and a one follows a zero, that is, the only sequences of inputs of concern are those of the form 0101 $\cdots$ and 1010 $\cdots$ applied to a start state q_1. Furthermore, the first two outputs from any sequence of inputs of interest are 0, 0.

At first glance it appears that $E_t = f(I_t\, E_{t-2}, E_{t-1})$. However, since a knowledge of which particular inputs $I = I_t$ are applicable to a state q depends on a knowledge of I_{t-1}, the output E_t depends on I_{t-1}; that is, $E_t = f(I_{t-1}, I_t, E_{t-2}, E_{t-1})$. In accordance with the general procedure, therefore, let q_1 be the start state and associate q_2 with the input 0 and q_8 with the input 1. Associate a distinct state for each triple $(I_{t-1}, E_{t-2}, E_{t-1})$. Thus associate q_4 with (0, 0. 0), q_5 with (1, 0, 0), q_6 with (0, 0, 1), q_7 with (1, 0, 1), q_8 with (0, 1, 0), q_9 with (1, 1, 0), q_{10} with (0, 1, 1), and q_{11} with (1, 1, 1). Then S is found to be as given in Fig. 6. A solution W to Problem Q for S is given in Fig. 7. It is obtained by letting $p_1 = \{q_1, q_2, q_6, q_8, q_9, q_{11}\}$, $p_2 = \{q_3, q_5, q_{10}\}$, and $p_3 = \{q_4, q_7\}$, p_1 being the start state. Then W is a minimal-state machine with respect to the original specifications.

Condition 2—For each set in a certain family of sets of input sequences, the desired machine is to be started

	0	1
q_1	q_2 0	q_3 0
q_2		q_5 0
q_3	q_4 0	
q_4		q_7 1
q_5	q_4 0	
q_6		
q_7	q_{10} 1	
q_8		q_6 0
q_9		
q_{10}		q_{11} 1
q_{11}	q_8 0	

Fig. 6—Machine S.

	0	1
p_1	p_1 0	p_2 0
p_2	p_3 0	p_1 1
p_3	p_2 1	p_3 1

Fig. 7—Machine W.

in some state (depending on the set of sequences). Either the outputs are to become meaningful, *i.e.*, satisfy (1), after max $\{r, s\}+1$ inputs; or it is to be assumed that the previous max $\{r, s\}$ input-outputs are known and the outputs are to become meaningful immediately.

It is readily seen that the synthesis technique may be successfully employed in those problems where the specifications satisfy (1) and condition 2. (The states of S are determined by the different sequences $I_{t-r}, \cdots, I_{t-1}, E_{t-s}, \cdots, E_{t-1}$.)

As an illustration of (1) and condition 2 consider the following problem.[5]

The machine desired satisfies condition 2. The inputs of interest are I^1, I^2, I^3, and the outputs are E^0, E^1, E^2, and E^3. The don't-care input sequences are all those in which at least one of the five pairs of inputs next listed occur in the order given.

$$I^1, I^1;\ I^2, I^2;\ I^2, I^3;\ I^3, I^3;\ I^3, I^2.$$

Suppose that $E_{t-1} = E^i$. If $I_t = I^1$ then $E_t = E^i$, if $I_t = I^2$ then $E_t = E^{i+1 \pmod 4}$ and if $I_t = I^3$ then $E_t = E^{i-1 \pmod 4}$.

Clearly $E_t = f(I_{t-1}, I_t, E_{t-1})$. To determine the states of S, associate a distinct state with each pair (I_{t-1}, E_{t-1}). Thus associate q_1 with (I^1, E^0), q_2 with (I^1, E^1), q_3 with (I^1, E^2), q_4 with (I^1, E^3), q_5 with (I^2, E^0), q_6 with (I^2, E^1), q_7 with (I^2, E^2), q_8 with (I^2, E^3), q_9 with (I^3, E^0), q_{10} with (I^3, E^1), q_{11} with (I^3, E^2), and q_{12} with (I^3, E^3).

[5] Modification of an example in [6], pp. 276–277.

Then machine S is constructed as given in Fig. 8. Machine W is given in Fig. 9, where $p_1=\{q_1, q_5, q_9\}$, $p_2=\{q_2, q_6, q_{10}\}$, $p_3=\{q_3, q_7, q_{11}\}$, and $p_4=\{q_4, q_8, q_{12}\}$. Machine W is a minimal-state machine with respect to the original specifications.

V. Unclocked Machines

In many physical (unclocked) machines, such as relay circuits and unpulsed electronic circuits, two consecutive identical signals AA (signal = input or output) are indistinguishable from the single signal A. For example, in an unclocked physical machine a steady, high input voltage usually cannot be distinguished from two consecutive, steady, high voltage inputs. A similar statement holds for outputs. In these situations, if input I produces output E, then $II=I$ produces $E=EE$. Also, $\delta(p, II)=\delta(p, I)$. In these instances it is customary to limit the machines under discussion solely to the unclocked ones, that is, only those machines where $\lambda(p, II)=EE$ and $\delta(p, I)=\delta(p, II)=\delta[\delta(p, I), I]$ whenever $\lambda(p, I)$ exists. This is done, for example, in [6] and [1]. In this section it will be shown that when the specifications are a modified form of those in Section III, the synthesis technique described in Section IV is applicable (in a slightly extended form) to unclocked machines.

Definition

A machine T is said to be *unclocked* if for each state p in T and each input I applicable to p, II is applicable to p, $\lambda(p, II)=EE$, and $\delta(p, I)=\delta(p, II)=\delta[\delta(p, I), I]$. A set of behavioral specifications is said to be *unclocked* if each time the specifications require an input I to yield an output E at a state p

1) the specifications require II to yield EE at p, and
2) the specifications for the output behavior at $\delta(p, I)$ are identical with the specifications at $\delta(p, II)$.

Two comments are in order at this point. First, in an unclocked machine, if $\lambda(q, I)$ exists then $\delta(q, I)$ exists. This follows from the fact that $\lambda(q, II)$ exists. Second, in view of the identical input-output specifications at the two states $\delta(p, I)$ and $\delta(p, II)$, it is clear that when synthesizing the machine S which satisfies a set of unclocked specifications in accordance with the procedure described in Section IV, S may always be selected to be unclocked.

Example 1

Find a minimal state machine which satisfies the following properties:

There is to be a start state. The inputs to the machine are 00, 01, 10, 11; and the outputs are 0 and 1. The don't-care input sequences are all those input sequences for which at least one of the four pairs of inputs next listed occur in the order given:

00, 11; 01, 10; 10, 01; 11, 00.

	I^1	I^2	I^3
q_1		q_6 E^1	q_{12} E^3
q_2		q_7 E^2	q_9 E^0
q_3		q_8 E^3	q_{10} E^1
q_4		q_5 E^0	q_{11} E^2
q_5	q_1 E^0		
q_6	q_2 E^1		
q_7	q_3 E^2		
q_8	q_4 E^3		
q_9	q_1 E^0		
q_{10}	q_2 E^1		
q_{11}	q_3 E^2		
q_{12}	q_4 E^3		

Fig. 8—Machine S.

	I^1	I^2	I^3
p_1	p_1 E^0	p_2 E^1	p_4 E^3
p_2	p_2 E^1	p_3 E^2	p_1 E^0
p_3	p_3 E^2	p_4 E^3	p_2 E^1
p_4	p_4 E^3	p_1 E^0	p_3 E^2

Fig. 9—Machine W.

For each sequence of inputs $\{I_j\}$ of interest let t_0 be the smallest integer t, having the property that there exist integers a and b, $a<b<t$, such that $I_a \neq I_b$ and $I_b \neq I_t$. For $t \geqq t_0$ let $r(t)$ and $s(t)$ be integers having the property that $I_{t-j}=I_t$ for $0 \leqq j < r(t)$, $I_{t-r(t)} \neq I_t$, $I_{t-r(t)-k}=I_{t-r(t)}$ for $0 \leqq k < s(t)$, and $I_{t-r(t)-s(t)} \neq I_{t-r(t)}$. For $t<t_0$ let $E_t=0$. For $t \geqq t_0$ let $E_t=1$ if and only if $I_{t-r(t)-s(t)}=00$, $I_{t-r(t)}=01$, and $I_t=11$; or $I_{t-r(t)-s(t)}=00$, $I_{t-r(t)}=10$, and $I_t=11$.

Since the specifications are unclocked, S may be selected to be an unclocked machine. Let q_1 be the start state. To provide for the outputs E_t when $t \leqq t_0$, associate q_2 with 00; q_3 with 01; q_4 with 10; q_5 with 11; q_6 with 00, 01; q_7 with 00, 10; q_8 with 01, 00; q_9 with 01, 11; q_{10} with 10, 00; q_{11} with 10, 11; q_{12} with 11, 01; and q_{13} with 11, 10. For $t \geqq t_0$ the output E_{t+1} depends only on $I_{t-r(t)-s(t)}$, $I_{t-r(t)}$, I_t, and I_{t+1}. To provide for the outputs E_t for $t>t_0$, associate a state with each possible distinct triple $(I_{t-r(t)-s(t)}, I_{t-r(t)}, I_t)$. Thus associate q_{14} with (00, 01, 00); q_{15} with (00, 01, 11); q_{16} with (00, 10, 00); q_{17} with (00, 10, 11); q_{18} with (10, 00, 10); q_{19} with (10, 00, 01); q_{20} with (10, 11, 10); q_{21} with (10, 11, 01); q_{22} with (01, 00, 01); q_{23} with (01, 00, 10); q_{24} with (01, 11, 01); q_{25} with (01, 11, 10); q_{26} with (11, 01, 11); q_{27} with (11, 01, 00); q_{28} with (11, 10, 11); and q_{29} with (11, 10, 00). Machine S, which is unclocked, is given in Fig. 10. A solution W to Problem Q for S is given in Fig. 11. It is

	00	01	10	11
q_1	q_2 0	q_3 0	q_4 0	q_5 0
q_2	q_2 0	q_6 0	q_7 0	
q_3	q_8 0	q_3 0		q_9 0
q_4	q_{10} 0		q_4 0	q_{11} 0
q_5		q_{12} 0	q_{13} 0	q_5 0
q_6	q_{14} 0	q_6 0		q_{15} 1
q_7	q_{16} 0		q_7 0	q_{17} 1
q_8	q_8 0	q_{22} 0	q_{23} 0	
q_9		q_{24} 0	q_{25} 0	q_9 0
q_{10}	q_{10} 0	q_{19} 0	q_{18} 0	
q_{11}		q_{21} 0	q_{20} 0	q_{11} 0
q_{12}	q_{27} 0	q_{12} 0		q_{26} 0
q_{13}	q_{29} 0		q_{13} 0	q_{28} 0
q_{14}	q_{14} 0	q_{22} 0	q_{23} 0	
q_{15}		q_{24} 0	q_{25} 0	q_{15} 1
q_{16}	q_{16} 0	q_{19} 0	q_{18} 0	
q_{17}		q_{21} 0	q_{20} 0	q_{17} 1
q_{18}	q_{16} 0		q_{18} 0	q_{17} 1
q_{19}	q_{14} 0	q_{19} 0		q_{15} 1
q_{20}	q_{29} 0		q_{20} 0	q_{28} 0
q_{21}	q_{27} 0	q_{21} 0		q_{26} 0
q_{22}	q_{14} 0	q_{22} 0		q_{15} 1
q_{23}	q_{16} 0		q_{23} 0	q_{17} 1
q_{24}	q_{27} 0	q_{24} 0		q_{26} 0
q_{25}	q_{29} 0		q_{25} 0	q_{28} 0
q_{26}		q_{24} 0	q_{25} 0	q_{26} 0
q_{27}	q_{27} 0	q_{22} 0	q_{23} 0	
q_{28}		q_{21} 0	q_{20} 0	q_{23} 0
q_{29}	q_{29} 0	q_{19} 0	q_{18} 0	

Fig. 10—Machine S.

	00	01	10	11
p_1		p_3 0	p_3 0	p_1 1
p_2	p_2 0	p_2 0	p_2 0	p_1 1
p_3	p_2 0	p_3 0	p_3 0	p_3 0

Fig. 11—Machine W.

obtained by letting $p_1 = \{q_{15}, q_{17}\}$, $p_2 = \{q_2, q_6, q_7, q_8, q_{10}, q_{14}, q_{16}, q_{18}, q_{19}, q_{22}, q_{23}, q_{27}, q_{29}\}$, and $p_3 = \{q_1, q_3, q_4, q_5, q_9, q_{11}, q_{12}, q_{13}, q_{20}, q_{21}, q_{24}, q_{25}, q_{26}, q_{28}\}$, with p_3 being the start state. Observe that the machine W determined, a minimal-state machine with respect to the original specifications, is unclocked.

In the above example the solution W to Problem Q for the unclocked machine S was unclocked. This was just a coincidence. In general, it is not true that if T is an unclocked machine, then each solution to Problem Q for T is unclocked.

Example 2

Let T be the unclocked machine in Fig. 12. Then machine W in Fig. 13 is a solution to Problem Q for T, with $p_1 = \{q_1\}$, $p_2 = \{q_2, q_4\}$, and $p_3 = \{q_2, q_3, q_5\}$. However, W is not unclocked since $\delta_W(p_1, I^1) = p_3$ and $\delta_W(p_1, I^1I^1) = p_2$.

This example shows that there may exist solutions to Problem Q for an unclocked machine which are not unclocked. Nevertheless, a solution can always be found which is unclocked. Specifically, there is the following algorithmic result.

Theorem 1

If T is an unclocked machine, then a V to Problem Q for T can always be found which is unclocked. Furthermore, for any solution W to Problem Q for T, an unclocked solution can always be found whose states are exactly the states of W (considering the states of W as sets of states of T).

Proof

Let W be a solution to Problem Q for T. Denote the states of W by $p_1, \cdots, p_h$. Each state p_i in W may be considered as a set $p_i = \{q_1{}^i, \cdots, q_{n^i(i)}\}$ of states of T. To prove the theorem it is sufficient to find a solution V containing just the states p_i, $1 \leqq i \leqq h$. To this end let p_a be any state of W. Write $p_1{}^a = p_a$. Suppose that I is an input and q an element of p_1^a such that $\lambda_T(q, I) = E$ exists. We shall define λ_V and δ_V for the state $p_1{}^a$ (possibly other states also) and the input I. To do this we shall first define, for each integer j, a state $p_j{}^a$ of W and a set $C_{j+1}{}^a$ of states of T. Therefore suppose that $p_j{}^a$ and

$$C^a_{j+1} = \{\delta_T(q, I) \mid q \text{ in } p^a_j, \lambda_T(q, I) \text{ exists}\}$$

are defined for each $j \leqq k$. Define $p_{k+1}{}^a$ to be the state $\delta_W(p_k{}^a, I)$ and $C_{k+2}{}^a$ to be the set

$$C^a_{k+2} = \{\delta_T(q, I) \mid q \text{ in } p^a_{k+1}, \lambda_T(q, I) \text{ exists}\}.$$

By mathematical induction, $p_j{}^a$ and $C_{j+1}{}^a$ become defined for each positive integer j. Clearly $C_{j+1}{}^a \subseteq p_{j+1}{}^a$[6] for each j. Let q be any element of $C_{j+1}{}^a$. Thus q is in $p_{j+1}{}^a$. From the definition of the set $C_{j+1}{}^a$, there exists an element q^* of $p_j{}^a$ such that $\lambda_T(q^*, I)$ exists and $\delta_T(q^*, I) = q$. Since $\lambda_T(q^*, II) = \lambda_T(q, I)$ exists and $\delta_T(q, I) = \delta_T(q^*, II) = \delta_T(q^*, I) = q$, q is in C^a_{j+2}. Thus

$$C^a_{j+1} \subseteq C^a_{j+2}$$

for each j. Thus $\{C_{j+1}{}^a\}_{j \geq 1}$ is an increasing sequence of states of T. Since T is finite, there exists a smallest in-

[6] For two sets A and B, by $A \subseteq B$ is meant that A is a subset of B.

	I^1	I^2	I^3
q_1	q_2 E^1		q_1 E^2
q_2	q_2 E^1		q_2 E^1
q_3	q_4 E^1		q_3 E^1
q_4	q_4 E^1	q_4 E^1	q_4 E^1
q_5		q_5 E^2	q_5 E^1

Fig. 12—Machine T.

	I^1	I^2	I^3
p_1	p_3 E^1		p_1 E^2
p_2	p_2 E^1	p_2 E^1	p_2 E^1
p_3	p_2 E^1	p_3 E^2	p_3 E^1

Fig. 13—Machine W.

teger, say s, such that $C_{s+1}{}^a = C_{s+2}{}^a$. Then

$$C_{s+2}^a = C_{s+1}^a \subseteq p_{s+1}^a.$$

Let $r(a)$ be the smallest integer such that $C_{r(a)+1}{}^a \subseteq p_{r(a)}$. In particular, $r(a) \leqq s+1$. For $i \leqq r(a)$, define $\lambda_V(p_i{}^a, I)$ to be E and $\delta_V(p_i{}^a, I)$ to be $p_{r(a)}{}^a$.

Repeat the above procedure in some systematic manner so that every state p in W and every input I is considered. It is now claimed that the states of W, together with δ_V and λ_V, form a machine V which is a solution to Problem Q for T. To see that V is a machine, it is necessary to verify that λ_V and δ_V are uniquely defined functions; that is, it does not ocur that $\lambda_V(q, I)$ or $\delta_V(q, I)$ is first defined to be one value and, later, to be a different value. This is obvious for λ_V. It is true for δ_V since, if $p = p_k^a$ for some a and some k, with $k \leqq r(a)$, $\delta_V(p, I)$ is determined solely by p and I. Since V has the same number of states as the solution W to Problem Q for T, in order to show that V is a solution to Problem Q for T it is sufficient to show that $T \leqq V$. This will follow from Theorem 1 of [10] if it can be shown that for each state p in V and each element q in p, if $\lambda_T(q, I)$ exists for an input I, then

1) $\lambda_V(p, I)$ exists and $\lambda_V(p, I) = \lambda_T(q, I)$, and
2) $\delta_T(q, I)$ is an element of $\delta_V(p, I)$.

But 1) and 2) are true from the way λ_V and δ_V were defined. Thus V is a solution to Problem Q for T which has the same states as W. This proves the theorem.

Remark

The above theorem may not be generalized in the obvious way to hold for sequences of inputs $II \cdots I$ of length $n > 2$. For example, let T be the machine given in Fig. 14. Then for each input I, if $\lambda_T(p, I)$ exists, then $\lambda_T(p, III)$ exists and $\delta_T(p, III) = \delta_T(p, II)$. However, the only solution to Problem Q for T is the machine W given in Fig. 15, where $p_1 = \{q_2, q_3, q_4\}$ and $p_2 = \{q_1, q_3, q_5\}$. In machine W there is no state p such that $\delta_W(p_1, I^1 I^1 \cdots I^1) = p$ for all sequences $I^1 I^1 \cdots I^1$ of arbitrarily high length. The theorem is still true if, in the definition of the unclocked machine, the output condition is modified to require only that $\lambda(q, II)$ exists whenever $\lambda(q, I)$ exists.

	I^1	I^2
q_1	q_2 E^1	q_1 E^1
q_2	q_3 E^1	q_2 E^2
q_3	q_3 E^1	
q_4	q_5 E^1	q_4 E^2
q_5	q_3 E^1	q_5 E^1

Fig. 14—Machine T.

	I^1	I^2
p_1	p_2 E^1	p_1 E^1
p_2	p_1 E^1	p_2 E^2

Fig. 15—Machine W.

	I^1	I^2	I^3
p_1	p_2 E^1		p_1 E^2
p_2	p_2 E^1	p_2 E^1	p_2 E^1
p_3	p_2 E^1	p_3 E^2	p_3 E^1

Fig. 16—Machine V.

To illustrate Theorem 1 let us apply it to Example 2. Let $p_1{}^1 = p_1$ and $I = I_1$. Then $C_2{}^1 = \{q_2\}$, $p_2{}^1 = p_3$, $C_3^1 = \{q_2, q_4\}$, $p_3{}^1 = p_2$, $C_4{}^1 = \{q_2, q_4\}$, and $C_4{}^1 \subseteq p_3{}^1$. Define $\delta_V(p_1, I^1) = p_2 = p_3{}^1$, $\lambda_V(p_1, I^1) = E^1$, $\delta_V(p_3, I^1) = p_2$, $\lambda_V(p_3, I^1) = E^1$, $\delta_V(p_2, I^1) = p_2$, and $\lambda_V(p_2, I^1) = E^1$. Next let $p_1{}^1 = p_1$ and $I = I^3$. Then $C_2{}^1 = \{q_1\}$ and $C_2{}^1 \subseteq \{p_1\}$. Define $\delta_V(p_1, I^3) = p_1$ and $\lambda_V(p_1, I^3) = E^2$. A continuation in the same manner yields the unclocked machine V of Fig. 16. Machine V is a solution to Problem Q for T and has the same states as W.

In view of the synthesis technique of Section IV and Theorem 1, the following three steps constitute a procedure which yields a minimal-state, unclocked machine Y satisfying a prescribed set of unclocked behavioral specifications.

1) Construct an unclocked machine S (satisfying the specifications) in accordance with Section IV.
2) Reduce S as much as possible to a machine W.
3) Apply Theorem 1 to obtain an unclocked machine Y with as many states as W.

VI. Conclusion

A technique has been presented for synthesizing *minimal*-state machines for large classes of behavioral specifications. A slight modification of this technique has been shown to be applicable for synthesizing minimal-state machines which have stability properties considered desirable when working with unclocked circuitry.

BIBLIOGRAPHY

[1] S. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y.; 1958.
[2] A. Church, "Application of Recursive Arithmetic to the Problem of Circuit Synthesis," presented at the Summer Inst. of Symbolic Logic, Cornell University, Ithaca, N. Y.; 1957.
[3] S. Ginsburg, "A synthesis technique for minimal state sequential machines," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 13–24; March, 1959.
[4] S. Ginsburg, "On the reduction of superfluous states in a sequential machine," *J. Assoc. Comp. Mach.*, vol. 6, pp. 259–282; April, 1959.
[5] S. Ginsburg, "A technique for the reduction of a given machine to a minimal state machine," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 346–355; September, 1959.
[6] D. A. Huffman, "The synthesis of sequential switching circuits", *J. Franklin Inst.*, vol. 257, pp. 161–190, 275–303; March/April, 1954.
[7] W. Keister, S. A. Ritchie, and S. Washburn, "The Design of Switching Circuits," D. Van Nostrand Co., Inc., New York, N. Y.; 1951.
[8] G. H. Mealy, "A method for synthesizing sequential circuits," *Bell Sys. Tech. J.*, vol. 34, pp. 1045–1079; September, 1955.
[9] E. F. Moore, "Gedanken experiments on sequential machines," in "Automata Studies," C. Shannon and J. McCarthy, Eds., Princeton University Press, Princeton, N. J., pp. 129–153; 1956.
[10] M. C. Paul and S. H. Unger, "Minimizing the number of states in incompletely specified sequential switching functions," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 356–366; September, 1959.
[11] J. M. Simon, "A note on memory aspects of sequence transducers," IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 26–29; March, 1959.

Arithmetic Operations for Digital Computers Using a Modified Reflected Binary Code*

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Summary—**The reflected binary or Gray code has been used chiefly in analog-to-digital conversion devices because its code sequences, representing any two consecutive integral numbers, differ in only one digit. This paper presents a method for performing the arithmetic operations of addition, subtraction, multiplication, and division using a modified reflected binary code.**

The modification for integral numbers is essentially the addition of an even parity check bit to the Gray code representation. This facilitates both the arithmetic operations and the detection of errors—in the arithmetic process as well as in transmission.

An adder using this code requires circuitry which is more complex than that of a conventional binary adder by a factor of about two or three. However, the adder can be used also for subtraction with little additional circuitry and without complementation. In applications where reliability requirements justify the extra circuitry needed for arithmetic error detection, the modified reflected binary code may compare favorably with the conventional binary.

INTRODUCTION

ELECTRONIC digital computers generally employ components having two distinguishable stable states. Although input data are commonly supplied in decimal form, numerical values in the computer are represented in some kind of binary code. So-called "binary" computers ordinarily translate an entire decimal number into its equivalent in the radix-2 number system. In "decimal" computers each decimal digit is individually replaced by a combination of binary digits in accordance with any one of various codes.

An important requirement of a code suitable for computational uses is that it lend itself readily to arithmetic operations. This paper shows how the "reflected binary" code devised by Gray[1] may be adapted to arithmetic computation. Gray's code has hitherto been used mainly in analog-to-digital conversion devices and associated circuitry[2] because its consecutive numbers differ in only one digit. In these applications the Gray code representation has been translated into the conventional binary or other code before being subjected to arithmetic manipulations.

The code to be presented here differs slightly from Gray's code. We shall designate it as the modified reflected binary (MRB) code. The MRB representation of an integer is the same as the Gray code representation except for the addition of one digit at the right end of the code word. This extra digit is, in effect, a parity bit chosen to give an even number of 1's in the code word. The addition of this digit facilitates both the arithmetic operations and the detection of any single errors either in transmission or in the arithmetic manipulations.

THE MRB CODE

Let the symbol A represent either a number or a code word equivalent to this number. Let A_k be the kth binary digit (from the right) of the binary code word A,

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[1] F. Gray, "Pulse code modulation," U. S. Patent No. 2,632,058; March 17, 1953.

[2] F. A. Foss, "The use of a reflected code in digital control systems," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-3, pp. 1–6; December, 1954.

with superscript b, g, or m to signify whether the word is in the conventional binary code, Gray's reflected binary code, or the modified reflected binary code, respectively. The digits of a Gray code word are related to those of the corresponding conventional binary word through

$$A_k^g = A_k^b \oplus A_{k+1}^b \qquad k = 1, 2, \cdots, K-1 \tag{1}$$

where $\oplus$ symbolizes addition modulo two, and $K-1$ is the number of digits in the binary word (so $A_K{}^b = 0$). MRB digits may be defined in terms of conventional binary digits by

$$A_k^m = A_{k-1}^b \oplus A_k^b \qquad k = 1, 2, \cdots, K \tag{2}$$

with $A_o{}^b = 0 = A_K{}^b$. Comparison of (1) and (2) shows that

$$A_k^m = A_{k-1}^g \qquad k = 2, 3, \cdots, K. \tag{3}$$

The MRB digits $A_2{}^m, A_3{}^m, \cdots, A_k{}^m$ are thus the same as the Gray code digits shifted one place to the left, and the digit $A_1{}^m$ is the same as $A_1{}^b$ (which is either 1 or 0 according to whether the number A is odd or even, respectively).

The inverse transformation from MRB to conventional binary is easily established. From (2),

$$A_k^b = A_k^m \oplus A_{k-1}^b.$$

Replacing $A_k{}^b{}_{-1}$ by $A_k{}^m{}_{-1} \oplus A_k{}^b{}_{-2}$, then $A_k{}^b{}_{-2}$ by $A_k{}^m{}_{-2} \oplus A_k{}^b{}_{-3}$, etc., yields

$$A_k^b = A_k^m \oplus A_{k-1}^m \oplus \cdots \oplus A_1^m$$

or

$$A_k^b = \sum_{j=1}^{k}{}_2 A_j^m \qquad k = 1, 2, \cdots, K \tag{4}$$

where $\sum_2$ indicates summation modulo two. Since $A_K{}^b = 0$, letting $k = K$ in (4) shows that the number of 1's in any MRB code word is necessarily even.

Let us now consider the relationship between the sequence of digits $A_1, A_2, \cdots$ of a binary code word and the corresponding numerical value A. For the conventional binary code, A is given by the following summation:

$$A = \sum_{k=1}^{K-1} A_k^b 2^{k-h} \tag{5}$$

where h is a positive integer specifying the location of the binary point. (If A is an integer, $h = 1$.) A similar expression may be derived for the MRB code. Substituting $2^{k+1} - 2^k$ for 2^k in (5) gives

$$\begin{aligned} A &= \sum_{k=1}^{K-1} A_k^b (2^{k+1} - 2^k) 2^{-h} \\ &= 2^{-h}[A_1^b(2^2 - 2^1) + A_2^b(2^3 - 2^2) + \cdots \\ &\qquad + A_{K-1}^b(2^K - 2^{K-1})] \\ &= 2^{-k} \sum_{k=1}^{K} (A_{k-1}^b - A_k^b) 2^k \quad \text{with} \quad A_0^b = A_K^b = 0 \\ &= \sum_{k=1}^{K} (-1)^{A_k^b} (A_{k-1}^b \oplus A_k^b) 2^{k-h}. \end{aligned} \tag{6}$$

The last step is easily verified by considering all four possible pairs of values of $A_{k-1}{}^b$ and $A_k{}^b$. Using (2) and (4) in (6) yields

$$A = \sum_{k=1}^{K} (-1)^{\sum_{j=1}^{k}{}_2 A_j^m} A_k^m 2^{k-h}. \tag{7}$$

The terms for which $A_k{}^m = 0$ contribute nothing to the sum. The remaining terms (for which $A_k{}^m = 1$) have alternating signs because

$$\sum_{j=1}^{k}{}_2 A_j^m$$

alternates between 0 and 1 as the successive 1's of the code word are added. The highest power of two with a nonzero coefficient has a positive sign because the MRB code word contains an even number of 1's.

An alternative notation, which does not include in the summation those terms for which $A_k{}^m = 0$, is often convenient. Let $a_1, a_2, \cdots, a_N$ be the sequence of values of $k-h$ for which $A_k{}^m = 1$, beginning with the highest such value. The sum (7) then becomes

$$A = \sum_{r=1}^{N} (-1)^{r+1} 2^{a_r}. \tag{8}$$

Note that the terms of (8) are in the opposite order from those in (7); in (8) the sum begins with the highest power of two. If the digit positions or columns of the code are numbered 0, 1, 2, $\cdots$, toward the left from the binary point, and $-1, -2, \cdots$, toward the right from the binary point, then $a_1, a_2, \cdots, a_N$ are the numbers of the columns (beginning at the left) in which 1's appear in the code word.[3] Thus, for the MRB number

[3] The equation corresponding to (8) for the conventional binary code is

$$A = \sum_{r=1}^{N} 2^{a_r}.$$

That for the Gray code is

$$A = \sum_{r=1}^{N} (-1)^{r+1}(2^{a_r+1} - 1),$$

but this expression is valid only for integral numbers.

10110.1011, we have $a_1=4$, $a_2=2$, $a_3=1$, $a_4=-1$, $a_5=-3$, $a_6=-4$; and the numerical value A is $2^4-2^2+2^1-2^{-1}+2^{-3}-2^{-4}=13\frac{9}{16}$.

The MRB equivalent of a given number A may be obtained by choosing the columns in which 1's will be placed as follows:

		Column Number 6	5	4	3	2	1	0	−1	−2	−3	−4
$9 = 16 - 8 + 2 - 1$	=			1	1	0	1	1				
$19 = 32 - 16 + 4 - 1$	=		1	1	0	1	0	1				
$28 = 32 - 4$	=		1	0	0	1	0	0				
$47 = 64 - 32 + 16 - 1$	=	1	1	1	0	0	0	1				
$9/16 = 1 - 1/2 + 1/8 - 1/16$	=							1.	1	0	1	1
$2\ 3/8 = 4 - 2 + 1/2 - 1/8$	=					1	1	0.	1	0	1	
$2\ 15/16 = 4 - 2 + 1 - 1/16$	=					1	1	1.	0	0	0	1.

a_1 is the lowest integer such that $2^{a_1} > A$

a_2 is the lowest integer such that $2^{a_1} - 2^{a_2} \leq A$

a_3 is the lowest integer such that $2^{a_1} - 2^{a_2} + 2^{a_3} > A$

a_4 is the lowest integer such that $2^{a_1} - 2^{a_2} + 2^{a_3} - 2^{a_4} \leq A$

. . . . . .

a_i is the lowest integer such that

$$\sum_{r=1}^{i} (-1)^{r+1} 2^{a_r} \begin{cases} > A \text{ if } i \text{ is odd} \\ \leq A \text{ if } i \text{ is even.} \end{cases} \quad (9)$$

(The word "lowest" is to be interpreted as "least positive" or "most negative.") The sum converges toward A as i increases. The process terminates if, after N terms, the sum is exactly equal to A. In such cases N is always even because the equals sign is contained only in those formulas for determining exponents a_i in which i is even. The process will always terminate in this manner if A is an integer or if A can be written as a fraction (proper or improper) whose denominator is some power of two. (The same condition obtains for termination of a conventional binary representation.) If A is not such a number, or if computer capacity or other considerations require that the code representation be broken off before it terminates automatically, the approximation must always be such that N is even (in order to allow arithmetic operations to be performed).

This "round-off" is accomplished in the following way. The a's are found as described above, stopping when the lowest allowable column number is reached, and the corresponding sequence of 0's and 1's is set down. If the number of 1's is odd ($=n$), the lowest-numbered column in which a 1 appears (a_n) is noted. Then the digit in the next higher-numbered column is changed (from 0 to 1 or from 1 to 0). This either replaces 2^{a_n} in the sum by $2^{a_n+1}-2^{a_n}$ (if the change is from 0 to 1) or replaces $-2^{a_n+1}+2^{a_n}$ by -2^{a_n} (if the change is from 1 to 0). (Then N, the final number of 1's, equals either $n+1$ or $n-1$, respectively.) The resulting MRB number differs from A in value by not more than $2^{a_{\min}-1}$ where $a_{\min}$ is the lowest allowable column number.

Some illustrative examples of decimal numbers and their MRB equivalents are the following:

Procedure for Addition

We now describe a sequence of pencil-and-paper steps which yield the sum (S) of two addends (A and B) expressed in the MRB code. The method will then be illustrated with some examples using the particular numbers listed above. A proof to justify the procedure is presented in Appendix I.

1) The first step, after writing one addend below the other with binary points aligned in the usual fashion, is to group the 1's into pairs. Reading from right to left, column by column, we pair the 1's as they appear, ignoring the 0's. The grouping may be indicated by encircling the two 1's of each pair (see examples below). Three different types of pairs may be distinguished. A "horizontal pair" consists of two adjacent 1's in the same addend. A "vertical pair" comprises two 1's lying in the same column. A "diagonal pair" comprises two 1's which lie in different addends and also in different columns. The term "*ab* pair" will be used to designate any pair which is either vertical or diagonal (*i.e.*, which contains a 1 from A and a 1 from B). In cases where the second 1 of a pair must be chosen from two 1's in the same column, we take the 1 which is in the same addend as the first 1 of the pair (to form a horizontal rather than a diagonal pair).
2) Next we form the partial sum corresponding to each pair as follows:
   a) For a horizontal pair, the partial sum is to have 1's in the two columns occupied by the 1's of the pair. Zeros may be placed in any intervening columns.
   b) For a diagonal pair, the partial sum is to have 1's in the two columns occupied by the pair and also a 1 in the next column to the left of the leftmost 1 of the pair.

c) For a vertical pair, the partial sum is to have simply a 1 in the next higher-numbered column. (A zero may be placed in the column of the pair if desired. As will appear in the next step, this is equivalent to placing two 1's in the column of the pair.)

3) The sum S is then obtained through addition modulo two of the partial sums.

The following examples illustrate these steps.

$$\begin{array}{rl} A = & 1\ 1\ 0\ 1\ 1 = 9 \\ B = & 1\ 1\ 0\ 1\ 0\ 1 = 19 \\ \text{partial sums} & \begin{array}{l} 1\ 0 \\ 1\ 1\ 1 \\ 1\ 1 \\ 1\ 1 \end{array} \\ S = & 1\ 0\ 0\ 1\ 0\ 0 = 28 \end{array}$$

$$\begin{array}{rl} A = & 1\ 1\ 0\ 1\ 0\ 1 = 19 \\ B = & 1\ 0\ 0\ 1\ 0\ 0 = 28 \\ & \begin{array}{l} 1\ 0\ 1 \\ 1\ 1\ 0\ 1 \\ 1\ 0 \end{array} \\ S = & 1\ 1\ 1\ 0\ 0\ 0\ 1 = 47 \end{array}$$

$$\begin{array}{rl} A = & 1.\ 1\ 0\ 1\ 1 = 9/16 \\ B = & 1\ 1\ 0.\ 1\ 0\ 1\ 0 = 2\ 3/8 \\ & \begin{array}{l} 1\ 1 \\ 1\ 0\ 1 \\ 1\ 1 \\ 1\ 1 \end{array} \\ S = & 1\ 1\ 1.\ 0\ 0\ 0\ 1 = 2\ 15/16 \end{array}$$

Circuit Implementation of Addition

As in conventional binary addition, it is not necessary that the partial sums be written out explicitly while performing MRB addition with pencil and paper. One may write down the final sum directly with the aid of temporary mental storage of pertinent information. The same is true for a digital computer, the essential difference being in the form of information storage.

The basic adder unit of the computer operates on two digits at a time—the two digits of A and B lying in a single column, beginning with the rightmost column. The information which must be passed along from one column to the next (that is, from one addition interval to the next in serial operation or from one basic adder unit to the next in parallel operation) concerns the pairing of the 1's and the partial-sum carry to the next column when an *ab* pair is completed. This information may be conveyed by two binary digits, for which we shall use the symbols E and F. Fig. 1 shows the block diagram of a parallel adder. The superscript m is now omitted for convenience in the designation of the digits, since only the MRB code is under discussion. Each block denotes a basic adder unit (BAU) whose operation is defined by the rules of addition. The inputs E_0 and F_0 and the outputs E_K and F_K are not used in addition of positive numbers (except perhaps for indication of overflow), but will be used later for subtraction.

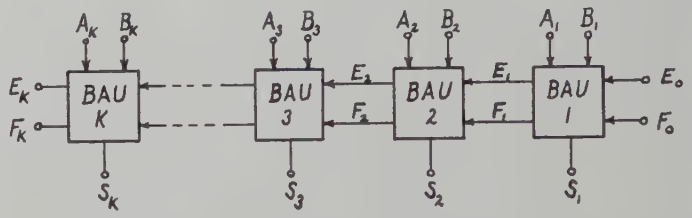

Fig. 1—Parallel adder.

There are four possible states with respect to the pairing of the 1's after each successive column has been inspected. These four states may be represented by the E and F digits as follows:

$E=1$ and $F=1$ indicates that an *ab* pair has just been completed and that a partial-sum 1 should be carried to the next column.

$E=1$ and $F=0$ indicates that the first 1 of the next pair has appeared in A.

$E=0$ and $F=1$ indicates that the first 1 of the next pair has appeared in B.

$E=0$ and $F=0$ indicates that the preceding pair (if any) has been completed, no carry is required, and the first 1 of the next pair has not yet appeared.

To illustrate, we consider again the addition of $A=11011$ and $B=110101$ as in the first example of the preceding section. In the least significant column are both 1's of an *ab* pair. The output digits of the first basic adder unit are therefore $S_1=0$, $E_1=1$, and $F_1=1$. The input digits of the next unit are $E_1=1$, $F_1=1$, $A_2=1$, and $B_2=0$. A_2 is the first 1 of the second pair, so $E_2=1$ and $F_2=0$. Regardless of whether the pair containing A_2 turns out to be horizontal or diagonal, its partial sum has a 1 in this column. Modulo-two addition of this 1 to the 1 carried from the previous column yields $S_2=0$. The input 1's to the third unit are E_2 and B_3. B_3 must be the second 1 of an *ab* pair; the output 1's are therefore S_3, E_3, and F_3. The input 1's to the fourth unit are E_3, F_3, and A_4—the same as for the second unit. The only output 1 is E_4. The input 1's to the fifth unit are E_4, A_5, and B_5. According to the rules, A_5 must complete a horizontal pair, and B_5 is the first 1 of the next pair. The partial sums for both these pairs have 1's in this column, so $S_5=0$. (Note that a carry indication and an indication that the first 1 of the next pair has appeared are never called for simultaneously because, when the second 1 of a pair and the first 1 of the next pair both lie in the same

column, the completed pair is always horizontal.) The input 1's to the sixth unit are F_5 and B_6; the only output 1 is S_6.

Table I gives the output digits (S_k, E_k, and F_k) of the basic adder unit corresponding to all possible combinations of input digits (E_{k-1}, F_{k-1}, A_k, and B_k). This table may be translated into a circuit diagram in any of several ways. The following equations[4] describe the table in terms of modulo-two addition and the AND operation (symbolized by ·).

$$\begin{aligned} S_k &= E_{k-1}\cdot F_{k-1} \oplus B_k \oplus A_k \\ E_k &= E_{k-1}\cdot F_{k-1} \oplus A_k \oplus E_{k-1} \\ F_k &= E_{k-1}\cdot F_{k-1} \oplus B_k \oplus F_{k-1}. \end{aligned} \tag{10}$$

A corresponding circuit configuration employing "half adders" and AND elements is shown in Fig. 2.

TABLE I

E_{k-1}	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
F_{k-1}	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
A_k	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B_k	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
S_k	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0
E_k	0	1	0	1	1	0	1	0	0	1	0	1	0	1	0	1
F_k	0	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1

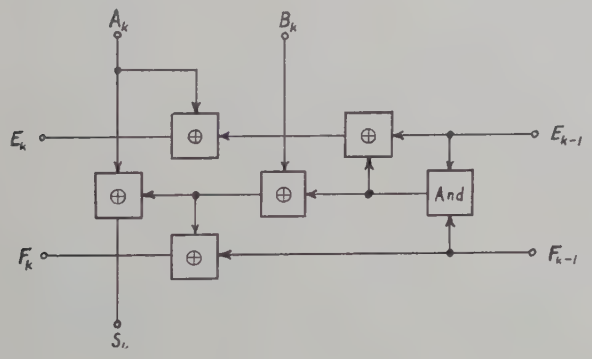

Fig. 2—Basic adder unit.

Subtraction

Subtraction may be performed with essentially the same pencil-and-paper procedure and the same circuitry as addition. The only difference is in the use of auxiliary 1's in the pairing process, or, equivalently, in the use of E_0, F_0, E_K, and F_K in the parallel adder of Fig. 1. In this section we describe the method. Proof of its validity is presented in Appendix III.

Assume first that the difference $D=A-B$ is desired and that $A\geq B\geq 0$. For purposes of pairing the 1's we imagine an extra 1 in the number A in some column to the right of the least significant actual column of A or B. This imaginary 1 is then paired with an actual 1 of A or B in the least significant column that contains a 1. This corresponds to inputs $E_0=1$ and $F_0=0$ to the first basic adder unit in the parallel adder. The procedure is then exactly the same as in addition. The leftmost 1 of A is paired with an imaginary 1 to the left of the leftmost column of A or B. This corresponds in the circuit to outputs $E_K=1$ and $F_K=0$ from the last basic adder unit. The partial-sum digits in the columns of the imaginary 1's are ignored.

To illustrate, we subtract 9 from 28 using the MRB code.

$$\begin{array}{rl} A = & 1\ 0\ 0\ 1\ 0\ 0 = 28 \\ B = & 1\ 1\ 0\ 1\ 1 = 9 \\ \hline & 1\ 1 \\ & 1\ 1\ 1 \\ & 1\ 1 \\ & 1 \\ \hline D = & 1\ 1\ 0\ 1\ 0\ 1 = 19. \end{array}$$

In many applications it is not known at the outset whether the subtrahend is smaller or larger than the minuend. If $B>A\geq 0$, the above procedure will not yield the correct difference directly. This situation can be detected in either of two ways: first, the E and F outputs from the final basic adder unit will be $E_K=0$ and $F_K=1$, indicating that the first 1 of the final pair has appeared in B rather than A; second, the resulting "difference" will contain an odd number of 1's, which is not possible with any correct MRB number. The correct difference may then be obtained either by repeating the process with inputs $E_0=0$ and $F_0=1$ to the rightmost basic adder unit instead of $E_0=1$ and $F_0=0$ or by simply changing one particular digit of the resulting difference (from 0 to 1 or from 1 to 0). The digit to be changed is the one immediately to the left of the least significant 1 of D. (The difference is, of course, negative in this case.)

The equivalence of these two correction procedures may be seen by observing that the least significant 1 of D lies in the rightmost column in which A and B have opposite digits (one 0 and one 1). The 1 of A or B in this column is shifted from a horizontal pair to a diagonal pair or from a diagonal pair to a horizontal pair as a result of reversing the inputs E_0 and F_0. Pairs to the left of this column are not affected by changing E_0 and F_0, and all pairs to the right of this altered pair are horizontal with either combination of E_0 and F_0. The only column of D affected by reversing E_0 and F_0 is the one containing the carry digit of the partial sum corresponding to the altered pair.

Negative numbers may be indicated by appending an additional sign digit, which we shall denote as σ, and letting $\sigma=0$ for negative numbers and $\sigma=1$ for positive numbers.

A combination adder and subtractor capable of handling both positive and negative numbers is shown in Fig. 3. "A," "O," and "I" denote AND, OR, and inverter elements, respectively, and a bar over a variable indicates inversion. The inputs are the digits of A and B, the signs of A and B, and control signals indicating

[4] These equations may also be derived independently of the pencil-and-paper procedure. This is done in Appendix II.

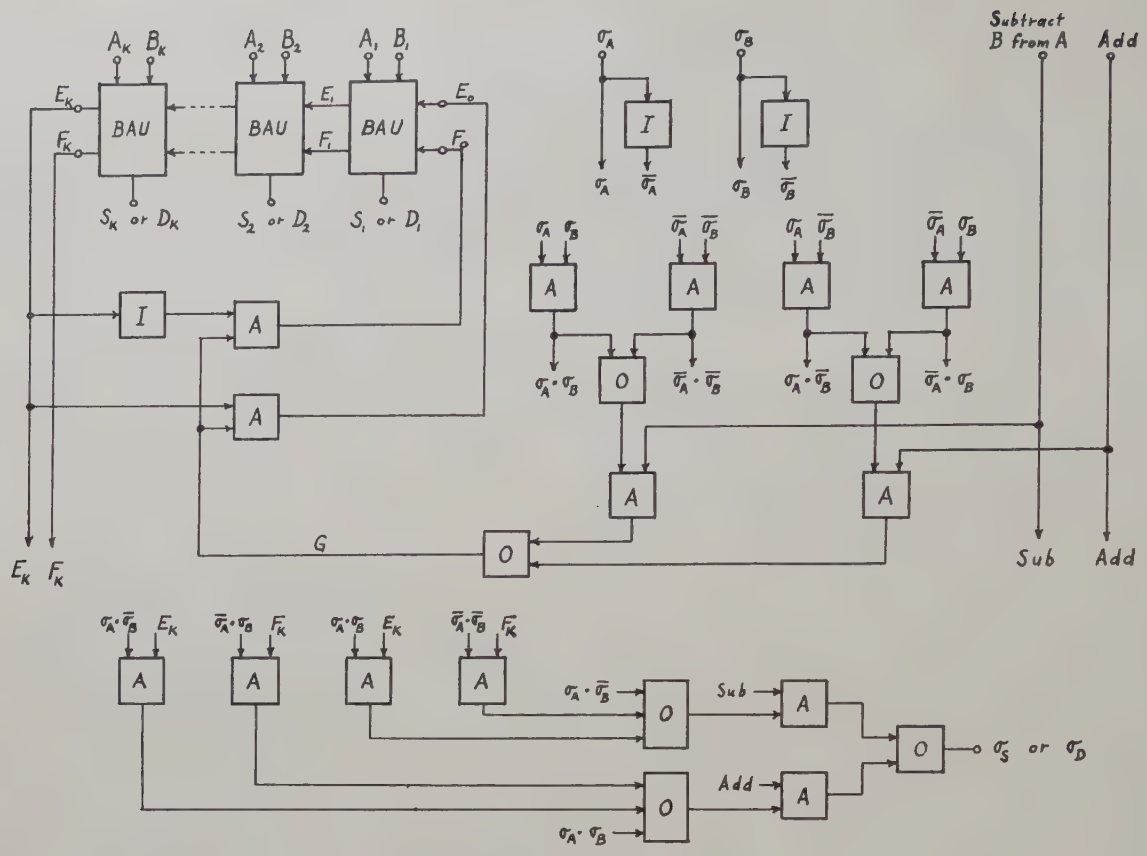

Fig. 3—Combination adder-subtracter.

whether B is to be added to or subtracted from A. The outputs are the sum or difference digits and the sign of the sum or difference.

The relative magnitudes of A and B are needed to determine both the output sign and the E_0 and F_0 inputs to the first basic adder unit when adding numbers of opposite sign or subtracting numbers of the same sign. These relative magnitudes are indicated by E_K and F_K. When $|A| > |B|$, then $E_K = 1$ and $F_K = 0$ (regardless of whether $E_0 = 1$ and $F_0 = 0$ or $E_0 = 0$ and $F_0 = 1$) and vice versa. (If $|A| = |B|$, E_K will be the same as E_0 and F_K the same as F_0.) $\overline{E}_K$ (rather than F_K) is used in the F_0 input circuit in order to initiate subtraction when both $E_K = 0$ and $F_K = 0$ (or $E_K = F_K = 1$).

The operation of this circuit may be described by the following Boolean equations in which $G = 1$ indicates that the difference of the magnitudes of A and B is required, add and sub refer to input addition and subtraction signals, respectively, and sums and products denote OR and AND operations, respectively.

$$\begin{aligned} G &= (\text{add}) \cdot (\sigma_A \cdot \bar{\sigma}_B + \sigma_A \cdot \bar{\sigma}_B) \\ &\quad + (\text{sub}) \cdot (\sigma_A \cdot \sigma_B + \bar{\sigma}_A \cdot \bar{\sigma}_B) \\ E_0 &= E_K \cdot G \\ F_0 &= \overline{E}_K \cdot G \\ \sigma_S \text{ or } \sigma_D &= (\text{add}) \cdot (\sigma_A \cdot \sigma_B + \sigma_A \cdot \bar{\sigma}_B \cdot E_K + \bar{\sigma}_A \cdot \sigma_B \cdot F_K) \\ &\quad + (\text{sub}) \cdot (\sigma_A \cdot \sigma_B \cdot E_K + \sigma_A \cdot \bar{\sigma}_B + \bar{\sigma}_A \cdot \bar{\sigma}_B \cdot F_K). \end{aligned} \tag{11}$$

The sum or difference digits are given by (10).

Multiplication and Division

Multiplication of an MRB number

$$A = \sum_{r=1}^{N_A} (-1)^{r+1} 2^{a_r}$$

by some power of two, say 2^{b_t}, simply shifts all 1's of A to the left b_t places. [If b_t is negative, the shift is to the right $(-b_t)$ places.] In equation form,

$$2^{b_t} A = 2^{b_t} \sum_{r=1}^{N_A} (-1)^{r+1} 2^{a_r} = \sum_{r=1}^{N_A} (-1)^{r+1} 2^{a_r + b_t}.$$

Multiplication of A by a number

$$B = \sum_{t=1}^{N_B} (-1)^{t+1} 2^{b_t}$$

is accomplished through alternate addition and subtraction combined with shifting:

$$\begin{aligned} AB &= A \sum_{t=1}^{N_B} (-1)^{t+1} 2^{b_t} \\ &= 2^{b_1} A - 2^{b_2} A + 2^{b_3} A - \cdots - 2^{b_{NB}} A. \end{aligned}$$

MRB division, like conventional binary division, is a lengthier process than multiplication. Consider division of A by B to obtain the quotient Q. We seek a number

$$Q = \sum_{r=1}^{N_Q} (-1)^{r+1} 2^{q_r}$$

such that N_Q is even and

q_1 is the lowest integer such that $2^{q_1} > A/B$ or $2^{q_1}B > A$,

q_2 is the lowest integer such that $2^{q_1} - 2^{q_2} \leq A/B$ or $2^{q_2}B \geq 2^{q_1}B - A$,

q_3 is the lowest integer such that $2^{q_1} - 2^{q_2} + 2^{q_3} > A/B$ or $2^{q_3}B > 2^{q_2}B - (2^{q_1}B - A)$, etc.

A procedure for finding Q is as follows:

1) Place B below A with binary points aligned. Then shift B to the position in which the leftmost 1's of A and B are aligned. Let k be the number of places by which B is shifted (positive for left shift, negative for right). It is necessarily true that

$$2^{k+1}B > A \quad \text{and} \quad 2^{k-1}B < A.$$

Consequently, q_1 equals either $k+1$ or k. To determine which, we subtract 2^kB from A. If the difference is negative, $q_1 = k$; if positive or zero, $q_1 = k+1$. Let $R_1 = 2^{q_1}B - A$. (If $q_1 = k+1$, R_1 may be obtained by subtracting 2^kB again from $A - 2^kB$ and changing the sign of the result.)

2) We now seek q_2, the lowest number such that $2^{q_2}B \geq R_1$. First we subtract $2^{q_1-1}B$ from R_1. The difference cannot be positive. If the difference is zero, $q_2 = q_1 - 1$ and the division process terminates (see step 3). If the difference is negative, we next subtract $2^{q_1-2}B$ from R_1. (This is equivalent to adding $2^{q_1-2}B$ to $R_1 - 2^{q_1-1}B$.) If $R_1 - 2^{q_1-2}B > 0$, $q_2 = q_1 - 1$ and we proceed to step 3. If $R_1 - 2^{q_1-2}B < 0$, then $q_2 < q_1 - 1$ and we next subtract $2^{q_1-3}B$ from R_1. If $R_1 - 2^{q_1-3}B > 0$, then $q_2 = q_1 - 2$ and we proceed to step 3. Otherwise, we subtract $2^{q_1-4}B$ from R_1. This continues until a positive difference is obtained.

3) Let $R_2 = 2^{q_2}B - R_1$. If $R_2 = 0$, the process has terminated and the remaining digit positions of Q should be filled in with zeros. Otherwise $R_2 > 0$. We next seek q_3, the lowest number such that $2^{q_3}B > R_2$. We first subtract $2^{q_2-2}B$ from R_2. (Subtracting $2^{q_2-1}B$ would always give a negative result.) If $R_2 - 2^{q_2-2}B \geq 0$, then $q_3 = q_2 - 1$ and we proceed to step 4. If $R_2 - 2^{q_2-2}B < 0$, we next subtract $2^{q_2-3}B$ from R_2 (or, equivalently, add $2^{q_2-3}B$ to $R_2 - 2^{q_2-2}B$). If $R_2 - 2^{q_2-3}B \geq 0$, then $q_3 = q_2 - 2$ and we go to step 4. Otherwise, we subtract $2^{q_2-4}B$ from R_2. This continues until a non-negative difference is obtained.

4) Let $R_3 = 2^{q_3}B - R_2$. This step proceeds exactly like step 2 except that subscripts on R's and q's are increased by 2. The following step is like step 3, the next like step 2 again, and so on.

The process continues until it terminates of itself or until the desired number of digits of Q is reached. The quotient may be rounded off to yield an even number of 1's as described earlier.

Summary and Evaluation

It has been shown that the arithmetic operations of addition, subtraction, multiplication, and division can be performed with the modified reflected binary code in a straightforward manner. The basic MRB addition process is more involved than its conventional binary equivalent because of the need for pairing the 1's of the addends. This requires that two bits of information be transmitted from each basic adder unit to the next instead of the single carry bit of conventional binary addition. It is difficult to make precise quantitative statements about the relative complexity of MRB and conventional binary circuits because this depends on the types of components used and the ingenuity of the circuit designer. However, the circuit diagrams presented here suggest that an MRB adder requires two to three times as many components as its conventional binary equivalent.

On the other hand, the MRB system has a few advantages which tend to offset the greater complexity of the basic adder. The adder can be used also for subtraction without need for complementing. The amount of extra circuitry in the combination adder-subtracter of Fig. 3, beyond that needed for addition of positive numbers alone, is approximately equal to that of a single basic adder unit.

Probably the greatest potential advantage is afforded by the error detection properties of the MRB code. Since all MRB numbers contain an even number of 1's, any error which affects only a single digit may be detected by counting the number of 1's. Parity checks of this sort are used extensively with the conventional binary code for detecting *transmission* errors, but detection of *arithmetic* errors requires considerable extra circuitry. In applications where reliability is important enough to justify the additional circuitry needed for detection of arithmetic errors, the MRB code may compare favorably with the conventional binary.

Appendix I

Our purpose here is to justify the hand computation procedure for performing MRB addition. Consider the addition of the numbers

$$A = \sum_{r=1}^{N_A} (-1)^{r+1} 2^{a_r} \quad \text{and} \quad B = \sum_{r=1}^{N_B} (-1)^{r+1} 2^{b_r},$$

where N_A and N_B are even, and

$$a_1 > a_2 > \cdots > a_{NA} \quad \text{and} \quad b_1 > b_2 > \cdots > b_{NB}.$$

We seek a way of writing the sum $S = A + B$ in the form

$$\sum_{r=1}^{N_S} (-1)^{r+1} 2^{s_r}$$

with N_S even and

$$s_1 > s_2 > \cdots > s_{N_S}.$$

Let the 1's of A and B be paired as described in the text. In the sum

$$S = A + B = \sum_{r=1}^{N_A} (-1)^{r+1} 2^{a_r} + \sum_{r=1}^{N_B} (-1)^{r+1} 2^{b_r}$$

each term of the right-hand member corresponds to one of the 1's of A or B. Let these terms be arranged in order of decreasing exponents and in such a way that adjacent terms may be paired corresponding to the pairing of the 1's.

To illustrate, we consider the following example:

$A =$ 1 1 0 0 1 0 0 1 1 1 = 285

$B =$ 1 0 1 0 1 0 1 0 1 1 0 0 = 1636

1 1

1 1

1 0 1

1 1 0 1

1 1

1 0 1

$S =$ 1 0 0 0 1 0 0 0 0 0 1 1 = 1921

$$S = A + B = (2^9 - 2^8 + 2^5 - 2^2 + 2^1 - 2^0) + (2^{11} - 2^9 + 2^7 - 2^5 - 2^3 - 2^2).$$

Rearranging the terms gives

$$S = (2^{11} - 2^9) + (2^9 - 2^8) + (2^7 + 2^5) + (-2^5 + 2^3) + (-2^2 - 2^2) + (+2^1 - 2^0).$$

Note that an even number of 1's of A and an even number of 1's of B must lie (in horizontal pairs) between successive ab pairs and to right of the rightmost ab pair. Furthermore, $2^{a_{N_A}}$ and $2^{b_{N_B}}$ are always prefixed by minus signs in their respective sums because N_A and N_B are even. Therefore the two terms of any ab pair are necessarily prefixed by the same sign; and the signs of successive ab pairs alternate, beginning with a minus sign for the rightmost ab pair. The two terms of any horizontal pair must have oposite signs, the sign of the higher-exponent term being the same as that of the next ab pair toward the right.

In order to cause the sequence of terms in the sum to have alternating signs throughout, let the higher-exponent term in each ab pair be replaced by the difference of two terms through use of the relationship

$$2^i = 2^{i+1} - 2^i.$$

In the example above, the sequence becomes

$$S = (2^{11} - 2^9) + (+2^9 - 2^8) + (+2^8 - 2^7 + 2^5) + (-2^5 + 2^3) + (-2^3 + 2^2 - 2^2) + (+2^1 - 2^0).$$

The exponents of the terms in each encircled group are now the column numbers of the 1's in the corresponding partial sum.

The sequence of exponents in the sum is still a monotonically nonincreasing sequence. It might at first appear that the substitution of the preceding paragraph could destroy this property. However, because of the preference given to a horizontal pair when the second 1 of a pair must be chosen from two 1's in the same column, the higher exponent of any ab pair must be less than the lower exponent of the next pair to the left. The substitution then gives, at worst, equal exponents in adjacent encircled groups of terms.

The sum is now expressed as an ordered sum of terms with alternating signs and monotonically nonincreasing exponents, and each term corresponds to a 1 in one of the partial sums. Adjacent equal-exponent terms (corresponding to two 1's in the same column in the array of partial-sum digits) cancel each other out. After such terms have been deleted, the remaining terms still have alternating signs, and the sequence of exponents is monotonically decreasing.

The number of ab pairs is necessarily even because 1) the total number of 1's in each addend is even, 2) each horizontal pair comprises two 1's from the same addend, and 3) each ab pair includes one 1 from each addend. The number of terms in the final sum is even because 1) the partial sum for every horizontal pair contains two terms, 2) there are an even number of ab partial sums, each containing an odd number (three) of terms, and 3) every cancellation of adjacent equal-exponent terms removes two terms. The final sum is therefore of the form

$$S = \sum_{r=1}^{N_S} (-1)^{r+1} 2^{s_r}$$

with N_S even and $s_1 > s_2 > \cdots > s_{N_S}$ as required. Furthermore, $s_1, s_2, \cdots s_{N_S}$ are the numbers of the columns in which 1's remain in the array of partial-sum digits after pairs of 1's in the same column have been cancelled out. They are, therefore, the column numbers of the 1's in a sum obtained through addition modulo two of the partial sums.

Appendix II

Eq. (10), which defines the MRB basic adder unit, may be derived directly without making use of the hand compution procedure.[5] This is accomplished by writing equations for the sum and carry digits in conventional binary code and applying (2) and (4) for translation between conventional binary and MRB.[6]

In the conventional binary code the sum digits are given by

$$S_k^b = A_k^b \oplus B_k^b \oplus C_{k-1}^b \qquad k = 1, 2, \cdots, K \qquad (12)$$

[5] The writer is indebted to a reviewer for several helpful suggestions including, in particular, this method of proof.

[6] Basic algebraic identities involving modulo two addition and the logical product are discussed by D. A. Huffman in "The synthesis of linear sequential coding networks," *Proc. Third London Symp. on Information Theory*; September 13, 1955.

where

$$C_k^b = A_k^b \cdot B_k^b \oplus (A_k^b \oplus B_k^b) \cdot C_{k-1}^b,$$

C_k^b is the kth carry digit, and $C_0^b = 0$. According to (2), the corresponding MRB sum digits are

$$S_k^m = S_{k-1}^b \oplus S_k^b.$$

Substituting from (12) gives

$$S_k^m = A_{k-1}^b \oplus B_{k-1}^b \oplus C_{k-2}^b \oplus A_k^b \oplus B_k^b \oplus C_{k-1}^b.$$

Rearranging the terms and again applying (2) gives

$$\begin{aligned} S_k^m &= A_{k-1}^b \oplus A_k^b \oplus B_{k-1}^b \oplus B_k^b \oplus C_{k-2}^b \oplus C_{k-1}^b \\ &= A_k^m \oplus B_k^m \oplus C_{k-1}^m, \end{aligned} \tag{13}$$

where

$$\begin{aligned} C_k^m &= C_{k-1}^b \oplus C_k^b \qquad (14) \\ &= C_{k-1}^b \oplus A_k^b \cdot B_k^b \oplus (A_k^b \oplus B_k^b) \cdot C_{k-1}^b \\ &= A_k^b \cdot B_k^b \oplus (A_k^b \oplus B_k^b) \cdot C_{k-1}^b \oplus C_{k-1}^b \cdot C_{k-1}^b \\ &= (A_k^b \oplus C_{k-1}^b) \cdot (B_k^b \oplus C_{k-1}^b). \qquad (15) \end{aligned}$$

The definition (14) implies, in the same way that (2) leads to (4), that

$$C_k^b = \sum_{j=1}^{k} C_j^m. \tag{16}$$

Substituting (4) and (16) into (15) gives

$$C_k^m = \left(\sum_{j=1}^{k}{}_2 A_j^m \oplus \sum_{j=1}^{k-1}{}_2 C_j^m \right) \cdot \left(\sum_{j=1}^{k}{}_2 B_j^m \oplus \sum_{j=1}^{k-1}{}_2 C_j^m \right).$$

If we define

$$\begin{aligned} E_k &= \sum_{j=1}^{k}{}_2 A_j^m \oplus \sum_{j=1}^{k-1}{}_2 C_j^m = E_{k-1} \oplus A_k^m \oplus C_{k-1}^m \\ F_k &= \sum_{j=1}^{k}{}_2 B_j^m \oplus \sum_{j=1}^{k-1}{}_2 C_j^m = F_{k-1} \oplus B_k^m \oplus C_{k-1}^m \end{aligned} \tag{17}$$

with $E_0 = 0$ and $F_0 = 0$, then

$$C_k^m = E_k \cdot F_k. \tag{18}$$

Substituting (18) into (17) and (13) gives the desired equations

$$\begin{aligned} E_k &= E_{k-1} \oplus A_k^m \oplus E_{k-1} \cdot F_{k-1} \text{ with } E_0 = 0 \\ F_k &= F_{k-1} \oplus B_k^m \oplus E_{k-1} \cdot F_{k-1} \text{ with } F_0 = 0 \\ S_k &= A_k^m \oplus B_k^m \oplus E_{k-1} \cdot F_{k-1}. \end{aligned} \tag{19}$$

Appendix III

The subtraction procedure may be justified by following either the line of reasoning of Appendix I or that of Appendix II. Choosing the latter course we seek the digits D_k^m of the difference D such that

$$D = A - B \quad \text{or} \quad A = B + D. \tag{20}$$

Applying (13) yields

$$A_k^m = B_k^m \oplus D_k^m \oplus C_{k-1}^m$$

or

$$D_k^m = A_k^m \oplus B_k^m \oplus C_{k-1}^m \tag{21}$$

where, according to (14),

$$C_k^m = C_k^b \oplus C_{k-1}^b,$$

and, from (12),

$$C_k^b = B_k^b \cdot D_k^b \oplus (B_k^b \oplus D_k^b) \cdot C_{k-1}^b.$$

Substituting (21) gives

$$\begin{aligned} C_k^b &= B_k^b \cdot (A_k^b \oplus B_k^b \oplus C_{k-1}^b) \oplus (A_k^b \oplus C_{k-1}^b) \cdot C_{k-1}^b \\ &= B_k^b \cdot (A_k^b \oplus 1) \oplus (A_k^b \oplus B_k^b \oplus 1) \cdot C_{k-1}^b. \end{aligned}$$

Therefore,

$$\begin{aligned} C_k^m &= B_k^b \cdot (A_k^b \oplus 1) \oplus (A_k^b \oplus B_k^b \oplus 1) \cdot C_{k-1}^b \oplus C_{k-1}^b \\ &= B_k^b \cdot (A_k^b \oplus 1) \oplus (A_k^b \oplus B_k^b \oplus 1) \cdot C_{k-1}^b \oplus C_{k-1}^b \cdot C_{k-1}^b \\ &= (A_k^b \oplus 1 \oplus C_{k-1}^b) \cdot (B_k^b \oplus C_{k-1}^b) \\ &= \left(1 \oplus \sum_{j=1}^{k}{}_2 A_j^m \oplus \sum_{j=1}^{k-1} C_j^m\right) \cdot \left(\sum_{j=1}^{k}{}_2 B_j^m \oplus \sum_{j=1}^{k-1} C_j^m \right) \\ &= E_k \cdot F_k \end{aligned} \tag{22}$$

where

$$\begin{aligned} E_k &= E_{k-1} \oplus A_k^m \oplus C_{k-1}^m \quad \text{with} \quad E_0 = 1 \\ F_k &= F_{k-1} \oplus B_k^m \oplus C_{k-1}^m \quad \text{with} \quad F_0 = 0. \end{aligned} \tag{23}$$

Substituting (22) into (21) and (23) gives

$$\begin{aligned} D_k^m &= A_k^m \oplus B_k^m \oplus E_{k-1} \cdot F_{k-1} \\ E_k &= E_{k-1} \oplus A_k^m \oplus E_{k-1} \cdot F_{k-1} \text{ with } E_0 = 1 \\ F_k &= F_{k-1} \oplus B_k^m \oplus E_{k-1} \cdot F_{k-1} \text{ with } F_0 = 0. \end{aligned} \tag{24}$$

Eq. (24) is the same as (10) or (19) except that $E_0 = 1$ for subtraction. This applies for $A > B$. If $B > A$, then A and B would be interchanged in (20), and (24) would be altered only in that $E_0 = 0$ and $F_0 = 1$.

It remains to be shown that if $A > B$, then $E_K = 1$ and $F_K = 0$ regardless of whether $E_0 = 1$ and $F_0 = 0$ or $E_0 = 0$

and $F_0=1$. From the procedure (9) for finding the a's and b's corresponding to given numerical values of A and B, it follows that if $A>B$, then $a_1 \geq b_1$. Furthermore,

$$\text{if } a_1 = b_1, \text{ then } a_2 \leq b_2;$$

$$\text{if } a_1 = b_1 \text{ and } a_2 = b_2, \text{ then } a_3 \geq b_3;$$

$$\text{if } a_1 = b_1,\ a_2 = b_2, \text{ and } a_3 = b_3, \text{ then } a_4 \leq b_4; \text{ etc.} \quad (25)$$

Let r_0 be the first value of r for which $a_r \neq b_r$. (Since $A>B$, the inequality must hold somewhere.) Let c_{r_0} be the larger of the two column numbers a_{r_0} and b_{r_0}. It is the number of the leftmost column in which the digits of A and B are not alike. An even number of 1's of A and B lie to the left of column c_{r_0}, and therefore an odd number of 1's must lie to the right of column c_{r_0} (since there is one 1 in column c_{r_0}, and A and B contain an even number of 1's altogether). One of the 1's to the right of column c_{r_0} is paired with the imaginary 1 corresponding to either $E_0=1$ and $F_0=0$ or $E_0=0$ and $F_0=1$. If the imaginary 1 is counted, there are an even number of 1's to the right of column c_{r_0}. Therefore the 1 in column c_{r_0} must be paired with a 1 to its left. Since $a_r=b_r$ for $r<r_0$, all pairs to the left of and including column c_{r_0} must be horizontal pairs. The number of 1's in these columns is odd, so one 1 will be left over after the pairing process (giving either $E_K=1$ and $F_K=0$ or $E_K=0$ and $F_K=1$).

If r_0 is odd, then $c_{r_0}=a_{r_0}>b_{r_0}$ and there are an even number of complete pairs in columns numbered c_{r_0} or higher. An example of this situation is the following:

$$\begin{array}{ll} A & (1)\ 0\ (1\ 1)\cdots \\ B & (1\ 0\ 1)\ 0\cdots. \end{array}$$

If r_0 is even, then $c_{r_0}=b_{r_0}>a_{r_0}$ and there are an odd number of complete pairs in columns numbered c_{r_0} or higher. This is illustrated by

$$\begin{array}{ll} A & (1)(1\ 0\ 0\ 1)\ 0\cdots \\ B & (1\ 1)\ 0\ 0\ (1\ 1)\cdots. \end{array}$$

In either case the left-over 1 is necessarily in A rather than B, which results in $E_K=1$ and $F_K=0$.

If $A=B$ and therefore $a_r=b_r$ for all r, then all pairs are horizontal. Since A and B each contain an even number of 1's, the two single 1's which are paired with imaginary 1's must be either both in A or both in B. This implies $E_K=E_0$ and $F_K=F_0$. An example is

$$\begin{array}{lll} A & (1)(1\ 0\ 1)(1) & (1\ 1)\ 0\ (1\ 1) \\ B & (1\ 1)\ 0\ (1\ 1) & (1)(1\ 0\ 1)(1) \\ & E_K = E_0 = 1 & E_K = E_0 = 0 \\ & F_K = F_0 = 0 & F_K = F_0 = 1. \end{array}$$

If $B>A$ the inequalities in (25) are reversed, and $E_K=0$ and $F_K=1$.

Magnetic Fields of Square-Loop Thin Films of Oblate Spheroidal Geometry*

H. CHANG† AND A. G. MILNES‡

Summary—**Thin films of Ni-Fe alloy may be prepared to be anisotropic and exhibit square-loop *M-H* characteristics. In films that are single-domained with flux changes involving only rotation of intrinsic magnetization controlled by cross-magnetization fields, very fast switching action can be obtained for storage and logic functions.**

Problems of coupling to the flux changes and interaction in an array of such films require study of the magnetic-field distribution. In the treatment given, a circular, single-domain, thin film is represented by a very flat oblate spheroid. The field distribution outside the spheroid is found by assuming that the magnetic properties are characterized by an intrinsic magnetization *M* constant in magnitude, but varies in direction depending on field and energy considerations.

Calculation of the field distribution is given for a typical film with diameter to thickness ratio of 10^5. From the regions over which field changes are most significant, conclusions are drawn as to the proper size of sensing loops and spacing to avoid interaction during switching in film arrays.

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I. Thin Films

REVERSAL of magnetization by coherent rotation in materials with uniaxial anisotropy (*i.e.*, a single preferred direction of magnetization), as suggested by Stoner[1] and others, has led to work on methods for preparing uniaxially anisotropic thin ferromagnetic films which exhibit such rotation.[2] Films are

[1] E. C. Stoner and E. P. Wohlfarth, "A mechanism of magnetic hysteresis in heterogeneous alloys," *Roy. Soc. London, Phil. Trans.*, vol. 240A, pp. 599–644; 1946–1948.

[2] M. S. Blois, Jr., "Preparation of thin magnetic films and their properties," *J. Appl. Phys.*, vol. 26, pp. 975–980; August, 1955.

made by electroplating or evaporating and depositing nickel-iron alloy on a flat plate. The thickness of a film is usually about 1000 Angstrom (or 10^{-5} cm), and the diameter may be 1 cm.

A film is single domained if its magnetization is uniform throughout its whole volume and rotates as a whole when subject to external field. It is quite conceivable that the film will behave as a single domain, since a magnetic field is applied in the plane of the plate during deposition to align all spins in the same direction and then strong spin coupling holds them together. Furthermore, the magnetization vector will always lie in the plane of the film since the demagnetizing factor (*i.e.*, the demagnetizing field per unit magnetization) is much smaller in the plane of the film than in the direction normal to the plane of the film.

Coherent rotation is a faster mechanism of flux reversal than domain-wall motion. Thus a thin film is inherently a faster switching device than a conventional ferrite core which reverses its magnetization by domain-wall motion. Moreover, as the two-dimensional configuration of a thin film lends itself to two cross-magnetic field controls, the film offers possibilities for logic operations. Vigorous investigations have been centered on materials, fabrication techniques, switching characteristics, mechanisms of switching, control of *M-H* loop shape, memory array design, device applications, etc.

In the present paper the field distribution outside a thin film is determined. Such knowledge is of importance in design since it allows determination of 1) the geometrical dimensions of a film in order to provide adequate flux and signal voltage, 2) the positions of driving and sensing windings in order to obtain proper excitation and detection, and 3) the spacing between films in an array in order to avoid interferences, and since it permits the computation of magnetic energy in the space caused by the presence of the film.

II. Mathematical Representations of Geometry and Magnetic Characteristics

An oblate spheroid rather than a cylindrical disk is taken as the geometrical model of a circular thin film. Since in spheroidal coordinates a single variable is adequate to specify the whole boundary surface of the film, this greatly simplifies solution of the problem.

The magnetic characteristic of the thin film is represented by

$$\overline{B} = \mu_0\overline{H} + \mu_0\overline{M} \tag{1}$$

where the magnetization $\overline{M}$ is constant in magnitude but dependent on the field intensity $\overline{H}$ in its orientation. For a film subject to a uniform field $\overline{H}$, the direction of $\overline{M}$ as a function of $\overline{H}$ can be determined by minimizing the total energy given by

$$E = -\mu_0\overline{M}\cdot\overline{H} + K\sin^2\theta \tag{2}$$

where the first term is the magnetization energy and the second is the anisotropy energy. K is the anisotropy constant, and θ is the angle between the magnetization $\overline{M}$ and the easy axis of magnetization produced during fabrication of the film. Slonczewski[3] and Bradley[4] independently have derived *M-H* characteristics which agree with experimental results when a film reverses flux by coherent rotation. Other experimental observations such as steps in ascending or descending branch in the *M-H* loops can be explained by assuming multiaxial anisotropy[5] for the films

$$E = -\mu_0\overline{M}\cdot\overline{H} + \sum_N K_N \sin^2 N\theta. \tag{3}$$

In (1) the term $\mu_0\overline{H}$ is much smaller than $\mu_0\overline{M}$ for all practical values of $\overline{H}$. Hence the actual value of the permeability is not important in determining the field. It is assumed to be air permeability (μ_0) in order that the fields due to exciting wire arrays and the fields of the ferromagnetic spheroid may be computed separately and independently except in the determination of the orientation of the magnetization. This is permissible since the magnetization of the film may be replaced by an equivalent current distribution without affecting the magnetic field. This results in actual and equivalent currents distributed in a homogeneous space of permeability μ_0, and thus allows use of the principle of superposition in separately calculating the fields due to currents and magnetization. The field of an actual current array may be found by using Biot-Savart's law; the field due to the magnetization may be found by the treatment that follows.

III. Magnetic Fields of Ferromagnetic Spheroid

A ferromagnetic spheroid, approximating a circular thin film, is shown in Fig. 1 in which *abcd* and *cdef* indicate two possible positions of sensing loop. The flux lines in the spheroid are all parallel from the assumption of uniform magnetization, and they travel in the air in

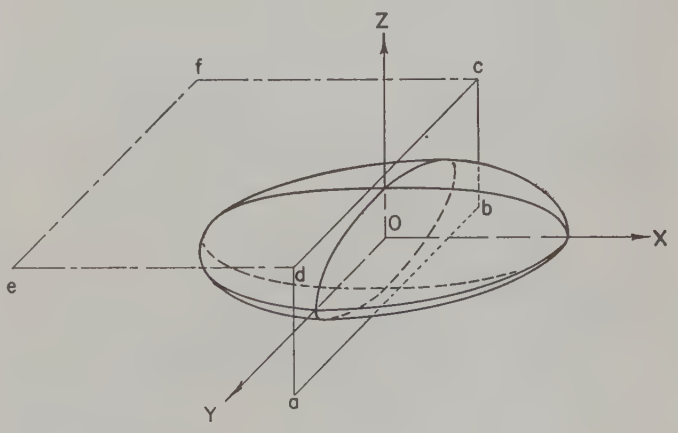

Fig. 1—Oblate spheroid approximating a circular thin film.

[3] J. C. Slonczewski, "Theory of Magnetic Hysteresis in Films and its Application to Computers," IBM Res. Lab., Poughkeepsie, N. Y., Res. Memo. No. 003.111,224; October 1, 1956.

[4] E. M. Bradley and M. Prutton, "Magnetization reversal by rotation and wall motion in thin films of nickel-iron alloys," *J. Electronics and Control* (*London*), ser. 1, vol. 6, pp. 81–96; January, 1959.

[5] R. E. Behringer, "Theory of Critical Curves and Hysteresis Loops in Thin Magnetic Films," IBM Res. Lab., Poughkeepsie, N. Y., Res. Memo. No. RC 63; October 30, 1958.

is the value of the ζ-coordinate representing the surface of the spheroid,

$$A = jH_{0x}f$$

$$C = \left\{ \frac{\mu_0 A\left[Q_1^1(j\zeta)\frac{d}{d\zeta}P_1^1(j\zeta) - P_1^1(j\zeta)\frac{d}{d\zeta}Q_1^1(j\zeta)\right]}{\mu Q_1^1(j\zeta)\frac{d}{d\zeta}P_1^1(j\zeta) - \mu_0 P_1^1(j\zeta)\frac{d}{d\zeta}Q_1^1(j\zeta)} \right\}_{\zeta_e} \tag{8}$$

and

$$B = \frac{P_1^1(j\zeta_e)}{Q_1^1(j\zeta_e)}\left(\frac{C}{A} - 1\right).$$

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directions approximately opposite to that in the spheroid in order to close their paths. When loop *abcd* fits closely around the spheroid, it links approximately all the flux lines in the magnetic material if the magnetization vector is along the X axis. However, if the magnetization is at an angle to the X axis, the loop links less flux. When the loop is made larger, the linkage with the return flux through the air will cancel part of the linkage with magnetization flux in the film. Loop *cdef*, when placed close to the film, links approximately half of the flux linked by loop *abcd*, since only half of the total flux lines close their path above the plane of symmetry X-Y.

We shall compute, from the potentials for a ferromagnetic spheroid, the field at a point external to the spheroid and the fluxes linking loops *abcd* and *cdef*.

As a convenient means of obtaining the potential functions of an oblate spheroid with uniform magnetization, we shall consider the following problem. An oblate spheroid of permeability μ and semiprincipal axes $a = b > c$ is embedded in free space μ_0. The axes a, b, c coincide with the coordinate axes X, Y, Z, respectively. Before the insertion of the spheroid, a uniform field H_{0x} was directed along the X axis of the spheroid. The results for the solution of the boundary value problem[6] are given below. The potential of the applied field is

$$P_0 = -H_{0x}X = -H_{0x}f[(1+\zeta^2)(1-\xi^2)]^{1/2}\cos\theta.$$
$$= AP_1^1(j\zeta)\,P_1^1(\xi)\cos\theta. \tag{4}$$

The presence of the spheroid disturbs the originally uniform field and the disturbed potentials are

$$P^+ = AP_1^1(\xi)[P_1^1(j\zeta) + BQ_1^1(j\zeta)]\cos\theta, \quad \zeta \geq \zeta_e \tag{5}$$

$$P^- = CP_1^1(\xi)P_1^1(j\zeta)\cos\theta, \quad \zeta \leq \zeta_e \tag{6}$$

where

$$\zeta_e = \sqrt{\frac{c^2}{a^2 - c^2}} \tag{7}$$

[6] H. Chang, "Fields Associated with Ellipsoids—with Applications to Shielding, Thin Films, and Twistors," Ph.D. dissertation, Elec. Engrg. Dept., Carnegie Inst. Tech., Pittsburgh, Pa.; February, 1959.

Hence the perturbation potentials, from (4)–(6), are

$$P_1^+ = P^+ - P_0 = ABQ_1^1(j\zeta)P_1^1(\xi)\cos\theta \tag{9}$$

$$P_1^- = P^- - P_0 = (C - A)P_1^1(j\zeta)P_1^1(\xi)\cos\theta. \tag{10}$$

The perturbation potentials, defined as the perturbed potentials minus the original potential of the applied field, arise from the induced magnetization in the oblate spheroid of permeability μ. From the internal perturbed potential (6), the internal field intensity is found as

$$\overline{H}^- = -\overline{\nabla}P^- = \frac{C}{A}H_{0x}\bar{i}_x \tag{11}$$

and is uniform both in magnitude $[(C/A)H_{0x}]$ and in direction (X direction) throughout the spheroid. Consequently, the induced magnetization defined as

$$\overline{M} = \frac{\mu - \mu_0}{\mu_0}\overline{H}$$
$$= \frac{\mu - \mu_0}{\mu_0}\frac{C}{A}H_{0x}\bar{i}_x \tag{12}$$

is also uniform both in magnitude and in direction throughout the spheroid. Thus the perturbation potentials P_1^+, P_1^- as found in (9) and (10) arise from uniform magnetization in the spheroid in the X direction. Since intrinsic and induced magnetizations should result in the same potentials if the magnetizations are of the same magnitude and direction, (9) and (10) also represent the potentials for a ferromagnetic oblate spheroid with uniform intrinsic magnetization in the X direction after substitution of

$$M_x = \frac{\mu - \mu_0}{\mu_0}\frac{C}{A}H_{0x}. \tag{13}$$

Therefore,

$$P_1^+ = M\frac{f\zeta_0(1+\zeta_0^2)}{2}Q_1^1(j\zeta)P_1^1(\xi)\cos\theta. \tag{14}$$

Since

$$P_1^1(\xi) = (1 - \xi^2)^{1/2} \tag{15}$$

and

$$Q_1^1(j\zeta) = (1 + \zeta^2)^{1/2}\left(\cot^{-1}\zeta - \frac{\zeta}{1 + \zeta^2}\right),$$

(14) may be rewritten as

$$P_1^+ = M\frac{a^2c}{2f^2}(1 + \zeta^2)^{1/2}\left(\cot^{-1}\zeta - \frac{\zeta}{1 + \zeta^2}\right) \cdot (1 - \xi^2)^{1/2}\cos\theta \tag{16}$$

where

$$f^2 = a^2 - c^2.$$

For rectangular coordinates,

$$H_t = -\frac{\partial P^+}{\partial t} = -\left(\frac{\partial P^+}{\partial \zeta}\frac{\partial \zeta}{\partial t} + \frac{\partial P^+}{\partial \xi}\frac{\partial \xi}{\partial t} + \frac{\partial P^+}{\partial \theta}\frac{\partial \theta}{\partial t}\right) \tag{17}$$

where

$$t = X,\ Y \text{ or } Z.$$

Hence for the case with magnetization in the X direction,

$$\frac{H_x}{-M_x\frac{a^2c}{2f^3}} = \left[\left(\cot^{-1}\zeta - \frac{\zeta}{1 + \zeta^2}\right) - \frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\cos^2\theta\right]$$

$$\frac{H_y}{-M_x\frac{a^2c}{2f^3}} = -\frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\cos\theta\sin\theta$$

$$\frac{H_z}{-M_x\frac{a^2c}{2f^3}} = -\frac{2\xi(1 - \xi^2)^{1/2}}{(1 + \zeta^2)^{1/2}(\zeta^2 + \xi^2)}\cos\theta. \tag{18}$$

Similarly, for the case with magnetization in the XY plane, at an angle θ_M with respect to the X axis, *i.e.*,

$$\overline{M} = M\cos\theta_M\,\bar{i}_x + M\sin\theta_M\,\bar{i}_y, \tag{19}$$

the normalized field intensities are

$$\frac{H_x}{-M\frac{a^2c}{2f^3}} = \cos\theta_M\left[\cot^{-1}\zeta - \frac{\zeta}{1 + \zeta^2} - \frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\cos^2\theta\right] + \sin\theta_M\left[-\frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\cos\theta\sin\theta\right]$$

$$\frac{H_y}{-M\frac{a^2c}{2f^3}} = \cos\theta_M\left[-\frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\cos\theta\sin\theta\right] + \sin\theta_M\left[\cot^{-1}\zeta - \frac{\zeta}{1 + \zeta^2} - \frac{2\zeta(1 - \xi^2)}{(1 + \zeta^2)(\zeta^2 + \xi^2)}\sin^2\theta\right]$$

$$\frac{H_z}{-M\frac{a^2c}{2f^3}} = \cos\theta_M\left[-\frac{2\xi(1 - \xi^2)^{1/2}}{(1 + \zeta^2)^{1/2}(\zeta^2 + \xi^2)}\cos\theta\right] + \sin\theta_M\left[-\frac{2\xi(1 - \xi^2)^{1/2}}{(1 + \zeta^2)^{1/2}(\zeta^2 + \xi^2)}\sin\theta\right]. \tag{20}$$

Note that ζ, ξ, and θ are dimensionless. H and M have the same dimensions so that H/M is dimensionless, and consequently

$$\frac{H}{M\,\dfrac{a^2c}{2f^3}}$$

is dimensionless. Hence (18) and (20) are normalized.

IV. Transformation from Spheroidal to Rectangular Coordinates

The expressions for field intensities as derived in Section III are in terms of spheroidal coordinates. However, since space can be more easily visualized and marked by rectangular coordinates, the discrete points at which the field intensity is to be found are therefore chosen in terms of rectangular coordinates. Oblate spheroidal coordinates and rectangular coordinates are related by the following equations:[7]

$$\frac{x^2+y^2}{1+\zeta^2}+\frac{z^2}{\zeta^2}=1$$

and

$$\frac{x^2+y^2}{1-\xi^2}+\frac{z^2}{-\xi^2}=1 \tag{21}$$

where

$$x=\frac{X}{f},\qquad y=\frac{Y}{f},\qquad z=\frac{Z}{f},$$

(x, y, z) are normalized coordinates, (X, Y, Z) are the original coordinates and f is one half the distance between the two foci. Then ζ^2 and ξ^2 can be found by solving (21), from which

$$\zeta^2=\frac{(x^2+y^2+z^2-1)+\sqrt{(x^2+y^2+z^2-1)^2+4z^2}}{2} \tag{22}$$

$$\xi^2=\frac{-(x^2+y^2+z^2-1)+\sqrt{(x^2+y^2+z^2-1)^2+4z^2}}{2}. \tag{23}$$

ζ is always positive and ξ has the same sign as z. The third coordinate θ is given by

$$\theta=\arctan\frac{Y}{X}.$$

V. Flux Linkage of Sensing Loops

For the loop *cdef* (see Fig. 1) at a distance $Z=Z_0$ above the XY plane, spanning from $X=-D$ to $X=0$ and from $Y=-L/2$ to $L/2$, the flux linking the loop is

$$\phi_z=\int_A \mu_0 H_z\,dX\,dY \qquad \left(\int_A \text{designates an area integral}\right)$$

$$=\mu_0\int_{X=-D}^{0}\int_{Y=-L/2}^{L/2} H_z\,dX\,dY,\ Z=Z_0. \tag{25}$$

Reference to (20) for H_z indicates that analytical integration of the above is impossible, hence resort must be made to numerical methods of integration. Since the limits of integration are constants, Gaussian-quadrature numerical integration can be used to advantage.

For the loop *abcd* (Fig. 1) lying in the XZ-plane and encircling the spheroid, the flux linking the loop is

$$\phi_x=\int_A B_x\,dA,\qquad x=0. \tag{26}$$

This integral is more difficult to handle than the preceding one for two reasons. First, B_x has different expressions for the inside and the outside of the spheroid.

$$B_x^- = \mu_0(M_x+H_x^-)=\mu_0(1-N_x)M_x \text{ (inside)}$$
$$B_x^+ = \mu_0 H_x^+ \text{ (outside)} \tag{27}$$

where N_x has been tabulated by Osborn[8] and the field intensity outside the spheroid, H_x^+, is given by (20). Hence the fluxes passing through the inside and the outside of the spheroid must be evaluated separately; namely,

$$\phi_x=\int_{A^-}\mu_0(1-N_x)M_x\,dA^- + \int_{A^+}\mu_0 H_x^+\,dA^+,\ x=0 \tag{28}$$

where the first integral is simply

$$\int_{A^-}\mu_0(1-N_x)M_x\,dA^- = \mu_0(1-N_x)M_x\int_{A^-}dA^-$$
$$=\mu_0(1-N_x)M_x\pi ac. \tag{29}$$

Second, a Gaussian-quadrature method of numerical integration applies only when both of the limits of integration in the double integral are constant. Since the inner boundary of the area A^+ is characterized by the spheroidal coordinate $\zeta=\zeta_e$, it is necessary to consider an elliptic loop ζ_2 instead of a rectangular loop to facilitate computation. Then

$$\int_{A^+}\mu_0 H_x^+\,dA^+ = 2\mu_0\int_{\zeta_e}^{\zeta_2}\int_{\xi=-1}^{1} H_x h_\zeta h_\xi\,d\zeta\,d\xi$$
$$=2\mu_0\int_{\zeta_e}^{\zeta_2}\int_{\xi=-1}^{1} H_x\left(f\,\frac{\xi^2+\zeta^2}{(1+\zeta^2)^{1/2}(1-\xi^2)^{1/2}}\right)d\zeta\,d\xi,$$
$$x=0 \tag{30}$$

where h_ξ and h_ξ are parametric constants in oblate spheroidal coordinates.

[7] *Ibid.*, p. 129.

[8] J. A. Osborn, "Demagnetizing factors of the general ellipsoid," *Phys. Rev.*, vol. 67, pp. 355–356; June 1 and 15, 1945. See Figs. 1–3.

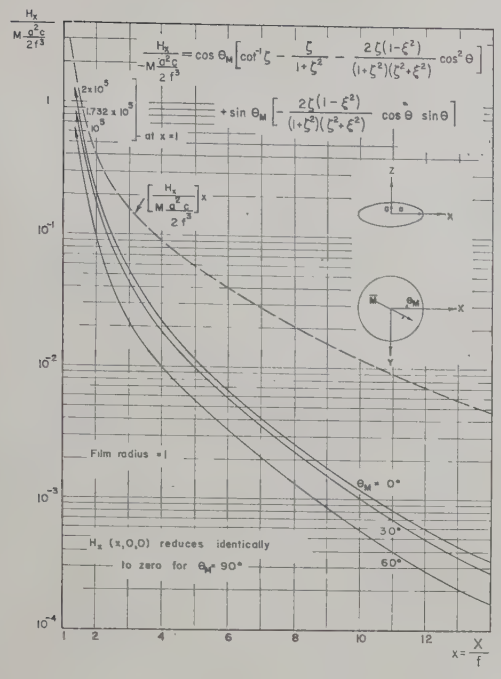

Fig. 2—Field strength H_x along the X axis.

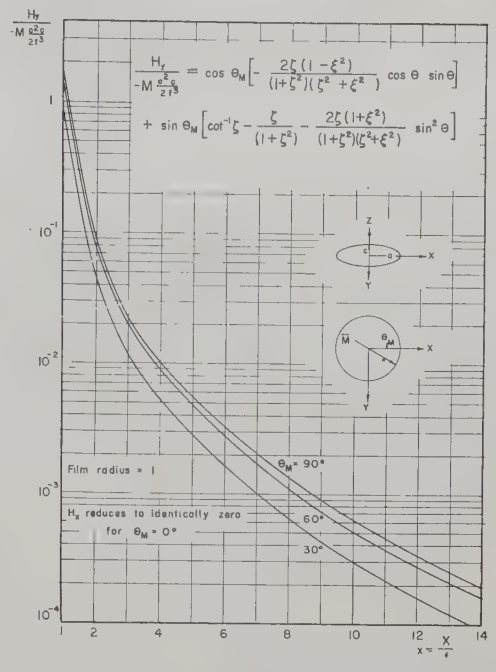

Fig. 3—Field strength H_y along the X axis.

VI. Sample Calculation and Discussion

For a film with diameter $2a = 1$ cm and thickness $2c = 1000$ Angstrom (10^{-5} cm), approximated by an oblate spheroid of major-to-minor-axes ratio $a/c = 10^5$, (20) has been employed to calculate the field intensities 1) along the X axis, for $X = a$, $2a$, 2^2a, etc., and 2) along the Z axis, for $Z = c$, $10c$, 10^2c, etc. It has been assumed that the magnetization vector M, lying in XY plane, is oriented with respect to the X axis at 0° to 90° at successive increments of 10°.

Since the field-intensity expressions are normalized, the results obtained, Figs. 2–4, apply to any value of the intrinsic magnetization M and the physical size, provided a/c is 10^5.

Examination of Figs. 2 to 4 leads to the following conclusions:

1) As the precipitous decrease of H_x with x in Fig. 3 suggests, the flux lines emanating from the film bend over in the immediate vicinity of the film and complete their return paths over and above the surfaces of the film.

If the magnetization of a film is conceived as a magnet, the rotation of the magnetization during switching can be considered as mechanical rotation of the magnet, with the flux lines emanating from the film rotating together. The lines radially farther away from the center of the film are sweeping through the space at a higher speed than that of the inner lines since the translational speed is proportional to the radial distance. As a consequence, the farther lines are more effective in inducing voltage during switching. A quantity more indicative of the effectiveness in inducing voltage should be $H_x x$ which is plotted in Fig. 2 as a dotted line. This quantity still decreases precipitously with x. From Fig. 2, at $x = 2$ (*i.e.*, one film-diameter's distance from the center), $H_x/M(a^2c/2f^3)$ is of the order of magnitude of 1, from which, since $f \cong a$, the ratio of flux densities outside and inside a film, $\mu_0 H_x/\mu_0 M$ is of the order of magnitude of $c/a = 10^{-5}$. Thus, despite the fact that at larger x the flux lines are sweeping at higher speed during switching, the induced voltage in a yz-plane loop placed at $x = 2$ is still much smaller than that caused by rotating magnetization in a yz loop of the same dimension placed at $x = 0$. Therefore, we conclude that in a film array, films can be deposited in a plane adjacent to one another (say, with a distance between the centers of neighboring films equal to 4a) without resulting in significant interference voltage from switching magnetization.

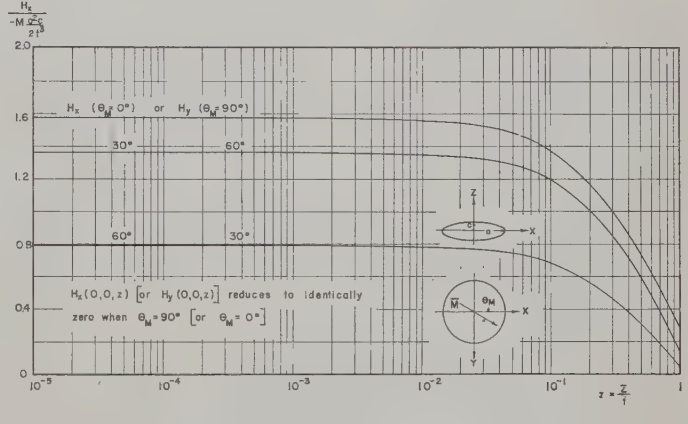

Fig. 4—H_x or H_y along the Z axis. (Calculated for a film thickness $C = 10^{-5}\ a \cong 10^{-5}\ f$.)

2) Along the z axis (Fig. 4), up to $z/f=10^{-1}$, the normalized field intensity in the X direction is about unity, namely

$$\frac{H_x}{-M\,\dfrac{a^2c}{2f^3}} \cong 1.$$

Hence the ratio of flux densities outside and inside the film, $\left|\mu_0 H_x/\mu_0 M\right|$, is about 10^{-5}. Therefore a loop around the film such as *abcd* in Fig. 1 can have considerable clearance between the wire and the film without the air flux cancelling out the magnetization flux significantly. For example, for a film with a cross-sectional area πac and a loop with area say, $2a\times a/50$, the air flux linked by the loop is roughly 1/100, *i.e.*,

$$\left(\frac{2a\,\dfrac{a}{50}\,\mu_0 H_x}{\pi ac\mu_0 M}\right)$$

that of the magnetization flux linkage.

3) Although only field intensity variations along the x and the z axes are computed in the sample calculation, (20) may be employed to calculate the field intensity anywhere external to the film. Without carrying out such calculation, we shall, in the light of boundary conditions and the calculated field intensities along the x and z axes, describe the field intensity distribution around the film.

Over the two flat surfaces of the film, the field intensity by the condition of continuity of tangential field intensity should be equal to the field intensity inside the film, which is

$$\overline{H}_i = -N\overline{M} \tag{31}$$

where N is the demagnetizing factor, *e.g.*,

$$\left(N = \frac{\pi}{4}\,10^{-5} \text{ for } \frac{a}{c} = 10^5\right).$$

As Fig. 4 indicates, the field intensity directly over the film is fairly uniform between

$$\frac{z}{f} \cong \frac{z}{a} = \pm\,10^{-1}.$$

The field intensity around the edge of the film can be found by the condition of continuity of normal flux density. At the film edge at an angle θ with respect to the magnetization vector, the radial field intensity H_r can be found from

$$\mu_0 H_r = B_{ir} = \mu_0(H_{ir} + M_r) \cong \mu_0 M\cos\theta;$$

hence

$$H_r = M\cos\theta. \tag{32}$$

As compared to the field intensity over the surface of the film ($NM=10^{-5}$M), the field intensity around the edge of the film ($M\cos\theta$) is much larger. However, the latter not only varies along the edge as $\cos\theta$, but also decreases precipitously with the radial distance beyond the film (see Figs. 2 and 3).

In device applications[9] where the field due to a neighboring film is not avoided as a detrimental interference, but utilized as an operating force, a detailed knowledge of the magnitude, direction and uniformity of the field distribution is necessary. Further details beyond the above general description can be obtained by using the field intensity equations.

4) The magnetic field distribution of an elliptic film of uniform intrinsic magnetization is solved[6] by an ellipsoidal geometrical representation of the film. Thus in principle the influence of elliptic film shapes can be found by using this solution, although the computation would be much more involved than the spheroidal case considered above.

VII. Acknowledgment

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[9] L. J. Oakland, "Coincident-current nondestructive readout from thin magnetic films," *J. Appl. Phys.*, suppl. to vol. 30, pp. 54S–55S; April, 1959.

Electrodeposited Twistor and Bit Wire Components*

S. J. SCHWARTZ† AND J. S. SALLO‡

Summary—Electrodeposition of ferromagnetic materials on wire is a suitable way of producing magnetic storage elements. One form of this element, when placed under suitable torsional strain (*i.e.*, as a twistor), has magnetic properties suitable for memory application. Through research into the electrodeposition process, a new device has been developed which requires no external stressing. This device has been designated as the "bit wire." The materials possess the desirable temperature stability usually associated with ferromagnetic metals and exhibit a high signal-to-noise ratio.

Both linear selection and coincident current memory arrays have been constructed with bit wire and plated twistors. The switching characteristics and drive requirements are similar for both materials. The significant difference lies in the fabricating technique, since the bit wire requires no stressing. Both devices are packaged, since undesired strains can change their properties. This problem has been minimized by plating the bit wire material on semirigid wire or tubing. The tubular structure offers other advantages, since additional sense, drive, or inhibit wiring may be threaded through the tube.

Introduction

A MAGNETIC device which utilizes a helical flux path along a cylinder was announced in 1957 by Bobeck [1]. In his original and subsequent papers [3], [4], he has described methods of constructing coincident-current memories with helical flux path devices (*i.e.*, twistors). Writing into the memory may be performed by passing currents through the twistor and through a solenoid around the twistor, such that the resultant magnetic field will switch irreversible flux along the helical direction of magnetization. Readout of stored information is performed by sensing across the twistor while pulsing the solenoid oppositely with a current sufficient to saturate the magnetic material in the opposite direction (Fig. 1).

The original twistors were either solid magnetic wire or wire plated with a magnetic coating and then drawn [2]. Subsequently, twistor operation has been achieved by using an oriented magnetic foil wrapped in a helix around a conducting wire [3]. Electrodeposition of a magnetic metal or alloy upon a conducting wire offers another means of preparing twistor-type devices. Through research, electrodeposited magnetic alloys have been developed which are fast switching, with square hysteresis loops when used as twistors.

Although the early plated twistors had very good properties, it was immediately obvious that twisting is an extra and expensive processing step in the production of "wire" memories. A research program initiated to produce components with a helical easy direction of magnetization has yielded the "bit wire" and the "bit tube" (Fig. 2). In these devices the helical path results only from the electrodeposition process. This process is of such a nature that the pitch of the helix can be varied. The bit wires, being the lower coercivity material, are more sensitive to stress than are twistors. This problem has been solved by plating the bit wire material on 0.010-inch to 0.015-inch wire or tubing. The larger diameter of the substrate means that the rod current must be increased for satisfactory coincident current writing. This disadvantage may be partially eliminated by changing the pitch of the helix to increase the circular flux efficiency at the expense of the axial flux efficiency.

The use of a tube instead of a wire permits the use of an isolated sense-line. This makes it possible to construct a coincident read coincident write array from an array fabricated similarly to a bit wire linear selection array. With a large enough tube, inhibit windings, bias windings, or windings for other functions can be passed through the tube, and thus versatility may be added to the component.

Linear-selection arrays have been made in both a flat bundle and a cable bundle using plated twistors. Flat bundle arrays have also been made of bit wire.

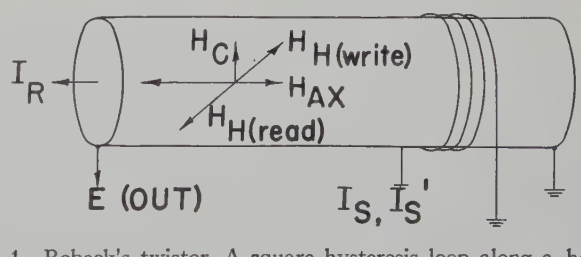

Fig. 1—Bobeck's twistor. A square hysteresis loop along a helical path (at 45° for wires under torsion) permits storage of one bit in the material under the solenoid due to coincident fields $H_{circular}$ and H_{axial}.

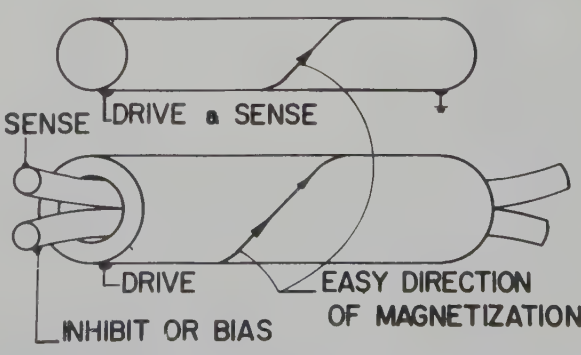

Fig. 2—Bit tubes and bit wires are devices produced with electrodeposition techniques which have a helical easy direction of magnetization due to the plating process.

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Materials Studied

The twistor and bit wire materials studied were electrodeposited alloys of iron-nickel and iron-nickel molybdenum. The materials for which data are reported in this paper are: 9 per cent Fe, 81 per cent Ni, 10 per cent Mo for twistors; and 22 per cent Fe, 78 per cent Ni, for bit wires.

Twistors are prepared by the continuous electrodeposition of the alloy on a 3-mil beryllium copper spring wire. The wire is pulled horizontally through several preplating steps, including a chemical cleaning, and finally is plated in a horizontal position and taken up on a reel. The cathode wire enters and leaves the plating vessels through small holes below the liquid level. The thickness of the magnetic deposit is controlled by the current density and the time of deposition and is in the range of 0.0001 inch to 0.0002 inch.

One of the advantages of the electrodeposition technique is the versatility of the process. Small changes in the plating bath or the deposition conditions will lead to significant changes in the magnetic properties of the deposit. Through judicious choice of variable combinations, it is possible to vary outputs, drive requirements, drive tolerances, required twist, and the alloy magnetostrictive characteristic.

One of the more important considerations is the substrate wire. The substrate has a large effect upon the magnetic properties of the deposit since the deposit structure and orientation are affected. This substrate effect has been used in the preparation of bit wires. A combination of a helically worked substrate and a specially developed plating bath leads to usable bit wire properties.

The continuous plating of bit wire is performed as follows: hardened wire, which has been straightened, is continuously taken off an eighteen-inch diameter reel and pushed through a tool which applies a helical microscratch to the surface of the wire. The wire continues through a plating process as previously described for the twistors and then passes through test coils by which the helical hysteresis response and pulse response are monitored. The final step is cutting the wires to length. The bit tube preparation is identical except that the tubing is available only in straight lengths under 30 feet long. This tubing can be purchased with or without isolated wire(s) through the center thus eliminating threading operations when tubing is used.

Both twistor and bit-wire materials are sensitive to strains which occur during normal handling. This is not a large factor in twistor fabrication since a large amount of externally induced stress is already present. However, in order to use the present bit wire material, it must be placed on the semirigid brass substrate.

The plating baths originally used for twistor and bit wire production were inherently unstable. It was found, however, that with suitable modification and control, long continuous lengths of material having uniform magnetic properties could be prepared. The yields are limited primarily by the quality of the substrate wire and its surface scratching, since pits, flat spots, and poor scratching cause spots of inferior magnetic material.

Component Properties

The electrical properties of interest to the engineer are the hysteresis properties of the materials, switching speeds, voltage outputs, ambient temperature effects, and signal-to-noise ratios when the materials are used as memory devices.

The flux change along the easy direction of magnetization (helical) produces the hysteresis loop upon which the twistor operation is based, and is different from the loop produced by observing axial or circular flux changes. Characteristic helical loops for the two materials are shown in Fig. 3.

The twistor loop shown has a B_r/B_m ratio of 0.95 and a coercivity of 10 oersteds when twisted 2.5 rad/cm. Increasing the twist to 5.0 rad/cm increases the coercivity to 12.5 oersteds and increases the B_r/B_m ratio. Breakage of the substrate wire occurs before maximum coercivity and squareness can be reached.

The bit wire loop of Fig. 3 is different in that the loop slope is negative when going from the remanence point to the knee. The flux switched before the knee is reversible. Some alloys tested also have some irreversible flux switched in the negative direction.

The slope of the hysteresis loop base is a function of at least two variables. First, as pointed out by Bobeck [1], the greater the helical strain anisotropy in the magnetic coating, the less switching can take place, due to the initial coherent rotation process; and second, the alloy and thickness of the plating can determine both the magnitude of the coherent rotation and its direction (*i.e.*, whether the hysteresis loop has a negative or positive slope from remanence to the knee).

The Fe-Ni-Mo twistors described showed no negative slope but twistors prepared of an iron-nickel alloy 78 per cent Ni to 22 per cent Fe had an appreciable negative slope which disappeared only under extreme stressing. Since the bit wires do not possess as strong a helical anisotropy as the plated twistors, alloy control must be

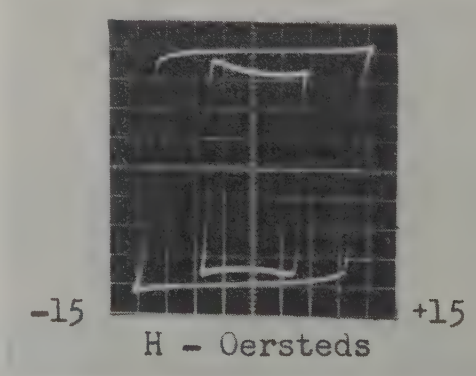

Fig. 3—Typical hysteresis loops measured at 2000 cps show the lower coercivity and differing shape of an inner-loop bit wire sample as compared with an outer-loop electrodeposited twistor

used to obtain the desired slope or initial permeability. High nickel alloys have a positive initial permeability while high iron alloys possess a negative initial permeability.

For linear selection memories, a negative slope is desired so that polarity discrimination can be used in the sense amplifiers instead of amplitude discrimination. Zero slope is desirable in coincident-current arrays where the polarity of readout is arbitrary.

Fast switching memory operation can be obtained with the plated materials being described. This results primarily from the high coercivities of the coatings (3 to 15 oersteds) coupled with reasonable switching coefficients. Others in the field are also working with high coercivity materials for memory applications using ferrites in various shapes and electrodeposited rods. The rods of Meier [5] are similar in operation magnetically to the materials being described except that their anisotropy is axial, not helical. It is felt that these devices can bridge the speed gap between conventional ferrite cores and thin films and thus serve in many applications.

The switching coefficients for various experimental twistors and bit wires have varied over a range of 0.6 to 5 oersted μsec. The bit wire and twistor being described have switching coefficients of 1.2 and 1.3 oersted μsec, respectively. The minimum fields required to switch to saturation (Fig. 4) were 6 and 15 oersteds, and since

$$T_{sw} = \frac{S_w}{H - H_O},$$

$$T_{sw} \cong \frac{1.2}{6 - 3.6} = 0.5 \ \mu\text{sec (bit wire)}$$

$$T_{sw} \cong \frac{1.3}{15 - 9} = 0.22 \ \mu\text{sec (twistor)}.$$

Another bit wire with a thinner deposit has a $S_w = 0.8$ and a H_O of 6.6 oersteds. For this material

$$T_{sw} = \frac{0.8}{11 - 6.6} \cong 0.18 \ \mu\text{sec (bit wire)}.$$

In the bit wire alloy region being described, the mode of switching is greatly affected by the plating thickness. A thick sample (0.0002) having a coercivity of 3 oersteds switches by wall motion processes at fields up to 2 H_c, while a thinner sample (0.00015) with a coercivity 6.6 oersteds will switch by incoherent rotation at fields of 7 oersteds to 2 H_c. The effects of alloy and thickness upon switching characteristics are now under investigation.

Output characteristic curves (Fig. 4) indicate the relative squareness of the materials under question. The curves were taken with the readout held constant to a saturating value so that the output voltage was a function of the flux set by the write current. Writing was done by setting flux with the rod current to allow accurate calculation of switching fields. The output characteristics apply directly to any linear-selection memory system in which the material is driven into saturation during a read operation and can be extended to true coincident-current application where full selection saturates the magnetic material. From these curves, operating write currents may be directly obtained to a particular current tolerance requirement.

As mentioned earlier, continuous twistors can be produced which are quite uniform. Results from a 1000-bit (5 bits/inch) sampling are shown in Fig. 5. The tests were conducted with current pulses adjusted to worst-case 10 per cent tolerances and indicate an average signal-to-noise ratio of 20:1. There were only four bits which had a $dV_z > 10$ mv (11, 12, 13, and 16 mv). The nominal operating currents for this twistor material are 200 ma and 100 ma for the rod and solenoid-write currents, respectively, with 300 ma solenoid-read current. The solenoid used during tests was 0.200 inch long (45 turns of no. 40 wire). Pulse risetimes were adjusted to 0.3 μsec.

The changes in twistor operation as temperature increases cannot be related to the normal changes in coercivity with temperature. Since a change in the strain anisotropy will occur as the substrate elongates or contracts, this can affect both the flux path helix angle and the coercivity. To minimize this, the externally induced

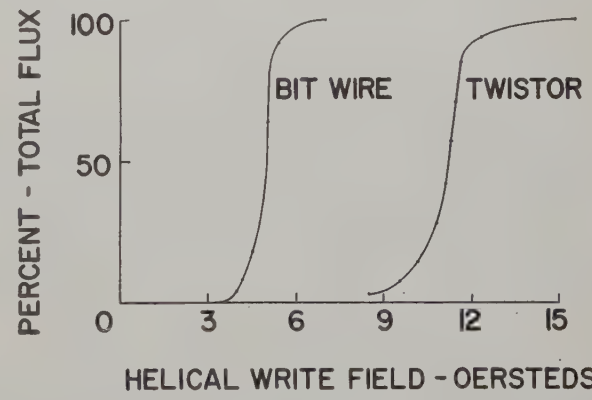

Fig. 4—Linear selection operation. Output characteristics like those above indicate the relative squareness of the material. Operating currents, current tolerances, and expected signal-to-noise ratios can be obtained from the curves.

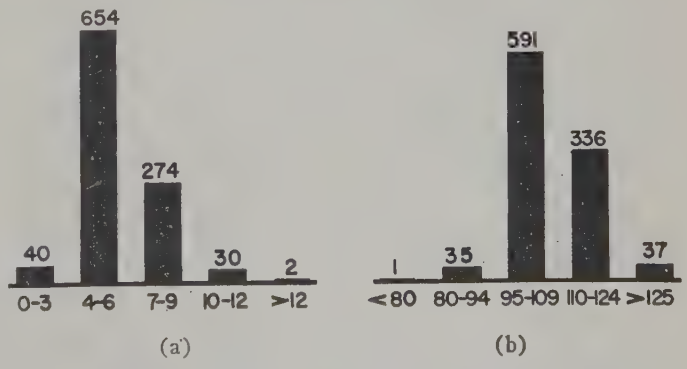

Fig. 5—Plated twistor uniformity, 1000-bit sampling. The output distributions show an average signal-to-noise ratio of 20 with a minimum over-all ratio of 8 for 995 bits. (a) dV_z-millivolts; (b) μV_1-millivolts.

strain must be large. The twistor material being described is capable of operation without temperature compensation over a 100°C range if very highly stressed (5 rad/cm or more). When lightly stressed, the temperature range can be much less. Temperature variations greater than this would require temperature compensation of memory-drive circuits. Since the variations with temperature result primarily from changes in the internal stress in both magnitude and angle, the corrections applied to the drivers providing the axial field will be different than those for the circular field drivers.

The bit wire temperature response is quite different from the response of an externally stressed twistor in that the helix angle is well established during the plating process. Tests at −100°C and +100°C have indicated that the squareness and the circular component of flux remain quite constant over this temperature range. Five per cent more circular field was required for switching at 100°C than −100°C, while the axial field required at 100°C was slightly less than at −100°C. Checks on the substrate wire have shown that it will twist with temperature variation and thus introduce additional stresses into the magnetic coating and a small change in helix angle. Fortunately, these stress changes are not large enough to seriously affect the bit-wire temperature characteristics.

Array Fabrication

When fabricating arrays from the plated twistor components, some means of securing and maintaining the desired twist must be provided. Since the thin electrodeposited coatings are strain sensitive to varying degrees, any packaging requires that little stress change be introduced into the magnetic coating by the packaging medium. This also suggests that to utilize the extreme temperature range of the device, the final package must not excessively alter the stress state of the magnetic element at any temperature in the desired usage range. Change of stress after packaging changes the hysteresis squareness from the stress state that existed before packaging, and can improve or reduce squareness. Two different types of arrays have been made with the twistor materials discussed.

The flat bundle is a potted-twistor array (Fig. 6). The twistors are stressed during testing, and acceptable elements are inserted directly into the array. A casting operation using epoxy resin fixes the ends of the twistor wires and maintains the twist. Before assembly, the twistors used in one array showed a minimum signal-to-noise ratio of 16 (using 10 per cent tolerance-worst-case currents). After assembly, this dropped to 9 (with the same current tolerances). This reduction in performance is primarily due to the change in length to diameter ratio between the test solenoid and the array solenoid.

Thirty-five of these arrays were constructed to study properties of this fabrication technique. The results showed that the epoxy maintained the desired stress but the assembly time is longer than desirable. Signal-to-noise ratios were very good except where twistors became unstressed during assembly.

In the cable-type bundle (Fig. 7), the stress is imparted to a group of twistors simultaneously to form a cable. This method offers a package with reduced solenoid inductance and resistance and a more desirable solenoid length to diameter ratio than is attainable with potted twistor arrays. The simultaneous twist technique is limited to plated twistors in a limited coercivity range and to cables with a moderately small number of twistors. More success was obtained with cable bundles by individually stressing each twistor.

Linear selection bit wire arrays similar to the flat bundle twistor arrays have been prepared. The use of the bit wire reduces testing costs since testing of bit wires is done as a final step in the continuous plating operation. A simple bit wire assembly technique has been worked out which consists of three steps. A grooved board is wound with the desired solenoids, the bit wires are slid into the grooves from the end, and the final step is connecting all lead wires to the proper terminals. Since the grooves are of sufficient width, no undesired strains are introduced into the platings by differences in expansion between the wire and the board. Tests on experimental bit-wire arrays have shown that signal-to-noise ratios are excellent due to the negative noise characteristic.

A method of making a conventional coincident-read coincident-write memory using two solenoids for selection was presented by Bobeck [1]. This form of array fabrication permits high field strengths at low currents but requires two solenoids per bit. Another type of array

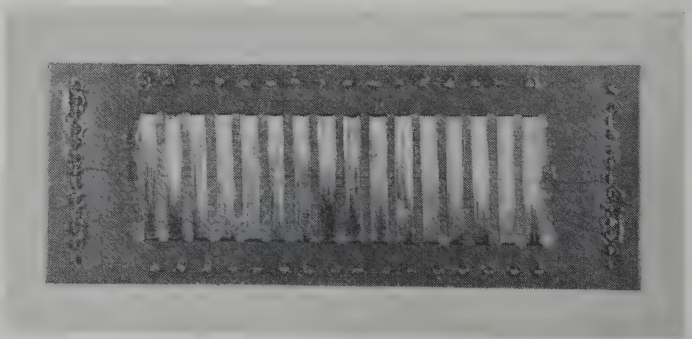

Fig. 6—Potted twistor array. Proper stress can be maintained in the plated twistors by potting them in epoxy. No appreciable change in magnetic properties has been attributed to the epoxy or any compression resulting from the epoxy solidifying.

Fig. 7—Cable twistor array. A group of plated twistors can be stressed simultaneously to form a compact memory array.

(Fig. 8) can be assembled to do this job using bit tubes as the magnetic element, thus permitting an isolated sense-line to thread through the array. This technique is suitable for small memories of a few hundred bits (*i.e.*, where two coordinate selection is satisfactory). Since only one solenoid is wound for Y_n bits, some fabrication savings are possible over the previously mentioned two-solenoid per bit fabrication. Temperature stability is the major gain of this type of memory over an equivalent ferrite core memory.

Because the sense line, though isolated, is always coaxial with a selected drive line, strobing in conjunction with delayed coincidence must be used (Fig. 9). This increases the cycle time over that required for bit wire linear selection memories, but due to the material switching speeds, cycle times compatible with core memories are easily obtained. This disadvantage can probably be eliminated by designing the array to cancel pickup between the Y lines and the sense. The hysteresis squareness requirements for the bit tubes are the same as for ferrite cores used in coincident current memories.

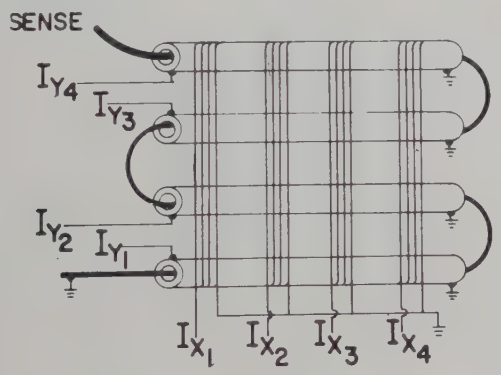

Fig. 8—Coincident current bit tube memory. The use of bit tubing allows isolation of the sense line from the drive lines and thus converts a linear selection array to a true coincident current array.

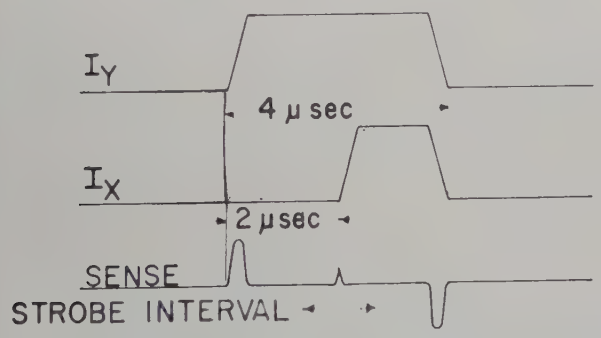

Fig. 9—Coincident current array waveforms. Since I_x generates a field perpendicular to the sense line, only the helical flux reversal in the bit tube magnetic coating induces a voltage on the sense line during the strobe time.

A 15-mil bit tube was used in coincident-read-write selection using a solenoid of 35 turns no. 34 wire (0.280 inch long). The easy direction of magnetization was a helix around the tube, 60° from the major axis of the tube. The write current on the tube (I_y) was 345 ma, and the write current on the solenoid (I_x) was 130 ma. I_x was delayed 2 μsec after the beginning of I_y and all pulses had a risetime of 0.2 μsec. Under these conditions, an output voltage of 24 mv was obtained with a disturbed zero reading of 1 mv. When currents were adjusted to 10 per cent tolerance-worst-case conditions, the ratio was 18/5. The major problem with this type of fabrication is keeping the rod current pulses quite flat during the peak value period to minimize the pickup on the sense line during the strobe interval. No attempt was made to optimize the operating speed.

Conclusions

Uniform plated twistors capable of high-speed, temperature-stable operation can be produced at low cost. A similar element which is much easier to fabricate into arrays, the bit wire, can be produced at approximately the same cost. The application will dictate which is selected as the device to be used.

Acknowledgment

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Bibliography

[1] A. H. Bobeck, "A new storage element suitable for large-sized memory arrays—the twistor," *Bell Sys. Tech. J.*, vol. 36, pp. 1319–1340; November, 1957.
[2] A. H. Bobeck, private discussion.
[3] A. H. Bobeck and R. S. Title, "The twistor—its use in a memory array," 1958 *Proc. Special Tech. Conf. on Nonlinear Magnetics and Magnetic Amplifiers*, Los Angeles, Calif., pp. 234–242; August 6–8, 1958.
[4] A. H. Bobeck and R. F. Fischer, "Reversible, diodless, twistor shift register," *J. Appl. Phys.*, suppl. to vol. 30, pp. 43S–44S; April, 1959.
[5] D. A. Meier, "A millimicrosecond magnetic switching and storage element," *J. Appl. Phys.*, suppl. to vol. 30, pp. 45S–46S; April, 1959.

Nondestructive Readout of Metallic-Tape Computer Cores*

L. M. LAMBERT†

Summary—The subject of this investigation is nondestructive readout of metallic-tape memory cores by the application of a magnetomotive force spatially in quadrature to the direction of remanent flux. A simple method of fabrication is proposed and empirical data for the design of the nondestructive read systems is obtained.

The use of nondestructive readout is not limited to digital computer circuits and no attempt has been made to use this method in any particular application; an experimental shift register was built, however, to test the method in a practical application. The nature of the system permits high-speed low-current-level operation in either digital or analog applications.

Introduction

THE use of toroidal ferromagnetic storage elements in information storage application is of considerable interest in telemetering[1,2] circuits, analog systems, and digital computers. The most undesirable aspect of such storage is the fact that no voltage or current levels are available to determine the state of such a device. In most practical applications, the state of the toroid or core is read by driving the core to one direction of remanent flux and observing whether an output occurs. If an output does occur, and if the original information is to be retained in storage, then the core must be reset to the original state. At the time of this investigation, several investigators[3–6] have proposed methods whereby this resetting action is not required because the core is not driven during reading, but merely examined electrically to determine its present state without destroying this state. These methods are generally classified as nondestructive readout systems. Buck and Frank[6] proved the feasibility of a method called quadrature field sensing; however, their experimental toroids were not well suited to fabrication with standard cores. The design proposed here, called circumferential turns sensing, is based on the quadrature field theory, but overcomes the practical difficulties of fabrication.

Quadrature Field Sensing

Quadrature Field Concept

A quadrature field is simply a magnetic field at right angles to the direction of remanent flux in a ferromagnetic material. Application of the quadrature field causes the remanent flux vector to tend to align itself with this field, thus rotating away from an easy direction toward a medium or hard direction as shown in planar representation in Fig. 1. If the quadrature field does not rotate the remanent flux vector past the hard direction, the flux will return to its original position of easy magnetization when the quadrature field is removed. The crystal strain energy and anisotropy energy oppose the change of residual flux away from the low-energy state of easy magnetization and also act to return the displaced vector to the original state.

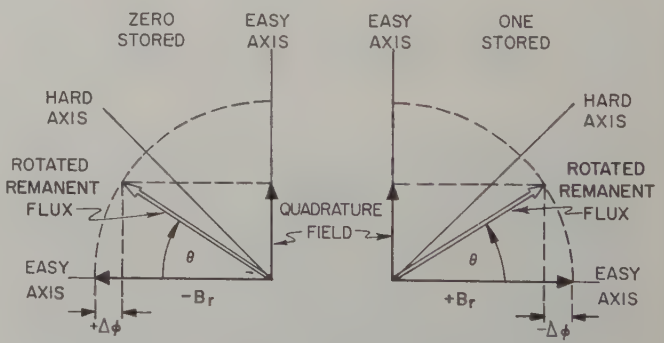

Fig. 1—Planar representation of quadrature field sensing of tape-wound computer cores.

In a polycrystalline ferromagnetic material there is a preferred or easy direction of magnetization which represents at least a statistical alignment of crystal easy directions. Actually the magnetic arrangement is not composed of single crystals, but of crystalline domains which have magnetic moments defined by direction, magnitude, and volume. It is more correct to say that the predominant domains are aligned in the preferred directions. Since the domains determine the actual flux vectors that rotate, it is reasonable to expect that the best amplitude of the quadrature field will depend on the magnetic moments of the domains. Thus, an opti-

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† Aeronutronic Div., Ford Motor Co., Newport Beach, Calif. Formerly with Electronics Res. Lab., University of California, Berkeley.

[1] W. Mathews, "Telemetering in earth satellites," *Elec. Engrg.*, vol. 76, pp. 976–981; November, 1957.

[2] C. B. House and R. L. Van Allen, "Commutation and Nondestructive Readout of Magnetic Memory Cores in Earth Satellites," presented at Natl. Telemetering Conf., Naval Res. Lab., Washington, D. C.; 1957.

[3] R. Thorensen and W. R. Arsenault, "A new nondestructive read for magnetic cores," *1955 Proc. WJCC*, pp. 111–116.

[4] V. L. Newhouse, "The utilization of domain wall viscosity in data-handling devices," PROC. IRE, vol. 45, pp. 1484–1492; November, 1957.

[5] B. Widrow, "A radio-frequency nondestructive readout for magnetic-core memories," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-3, pp. 12–15; December, 1954.

[6] D. A. Buck and W. I. Frank, "Nondestructive sensing of magnetic cores," *Trans. AIEE*, pt. 1, vol. 72, pp. 822–830; January, 1954.

mum value of quadrature field will rotate large domains very little while completely rotating smaller domains to a new direction of easy magnetization. The macroscopic result is a decrease in residual flux after the removal of the quadrature field. However, repeated application of the quadrature field will have no further effect on the large domains. Some domains may be rotated piecemeal by repeated application of the pulse.

For alloy metallic tapes, one axis of easy magnetization is within 10° of the direction of rolling in the milling process. Fig. 2 shows diagrammatically the effect of a quadrature field on the remanent flux of the tape as wound on a bobbin. It is evident that the original flux direction determines the sign of the change-of-flux quantity. Since B_r is essentially constant, the amplitude of a voltage induced in a winding around the core by this change of flux is inversely proportional to the rise time of the quadrature field.

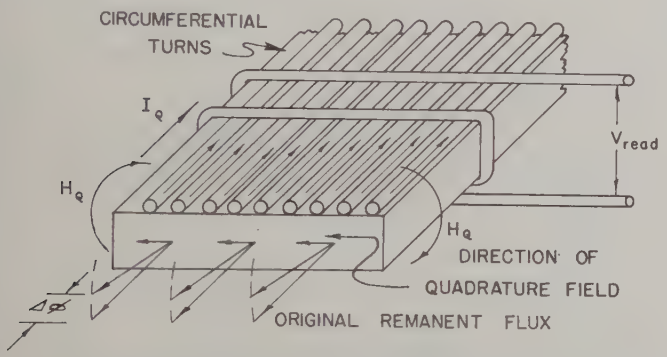


Fig. 2—Diagrammatical representation of the effect of the circumferential-turns quadrature field upon the remanent flux.

Circumferential Turns

Fig. 2 shows diagrammatically the fabrication of the circumferential turns and thus spatially quadrature field. This construction may be contrasted with the tape conductor construction and other suggestions of Buck and Frank.[6] As is evident, the turns are wrapped around the core bobbin in the same direction as the metallic tape itself. This fabrication was made using Supermalloy, 4-79 Mo-Permalloy, and Deltamax $\frac{1}{4}$-mil metallic tape of 6, 12, and 20 wraps on no. 15 ceramic bobbins. Several samples of each type of material were tested and the results showed reasonable agreement within each alloy type. Fig. 3 shows the typical waveforms for an 18-turn quadrature winding at a sensing level of about 5 ampere-turns with a 0.11-μsec rise time and a 10-turn read winding. One-sense operation as used in Fig. 3 is defined as the readout of a freshly magnetized core. The multiple-sense operation is the readout obtained after sensing the core for a large number of times, without remagnetizing the core. The tentative conclusions to be drawn from these waveforms are: 4-79 Mo-Permalloy is the most favorable material for multiple-sense operation, Supermalloy is unsatisfactory

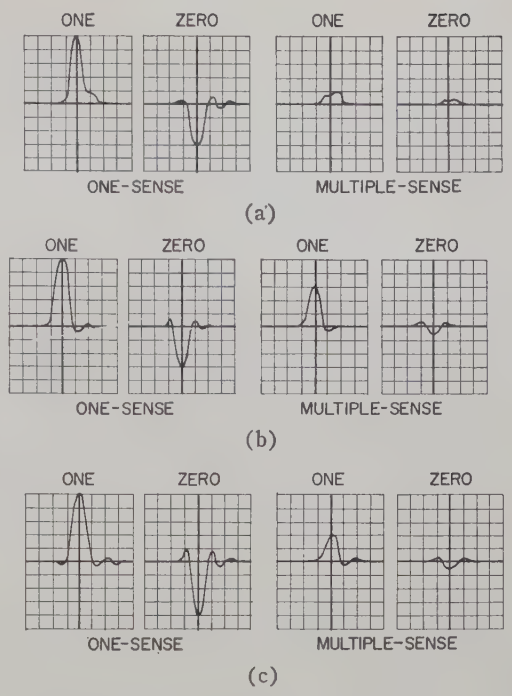


Fig. 3—Comparison of nondestructive readout signals from a 10-turn read winding with a value of quadrature field selected for a 1-volt output for a ONE. The vertical scale = 0.2 volt per division; the horizontal scale = 0.1 μsec per division. (a) 6 wraps of $\frac{1}{4}$-mil Supermalloy tape on no. 15 bobbin (5 per cent Mo, 79 per cent Ni, 17 per cent Fe). (b) 6 wraps of $\frac{1}{4}$-mil 4-79 Mo-Permalloy tape on a no. 15 bobbin (4 per cent Mo, 79 per cent Ni, 17 per cent Fe). (c) 6 wraps of $\frac{1}{4}$-mil Deltamax tape on a no. 15 bobbin (50 per cent Ni, 50 per cent Fe).

for multiple-sense operation, and one-sense operation is possible with all three materials.

The unsymmetrical outputs obtained in Fig. 3 are typical of the cores tested. Initially it was thought that the unsymmetrical output was due entirely to nonorthogonal coupling. However, this was checked carefully and although about 50 per cent of this dissymmetry in some cases was due to this coupling, there was also an unaccounted for dissymmetry. The dissymmetry, since it is not understood completely, will be shown in future curves, and the interpretation will be left to the individual reader.

Experimental Results

Confirmation of Theory

The following experimental observations which were obtained are in accordance with the proposed theory of quadrature field sensing.

The effect of quadrature pulse duration on nondestructive readout: a nominal pulse duration of 1.5 μsec was used for all quadrature sensing experiments. When the pulse duration was increased to 10 μsec, it was found to have no effect on either the loss of residual flux or the quadrature sensing output voltage.

The effect of quadrature pulse rise time on the sense voltage output is approximately proportional to rise

time of the quadrature drive pulse (for a given quadrature field).

The effect of multiple turns of quadrature winding have no significant effect on the conventional windings since the two sets of windings are at right angles. For a 25 or more turn quadrature winding (on no. 15 bobbin), inductive-capacitive effects may cause the quadrature drive pulse to oscillate.

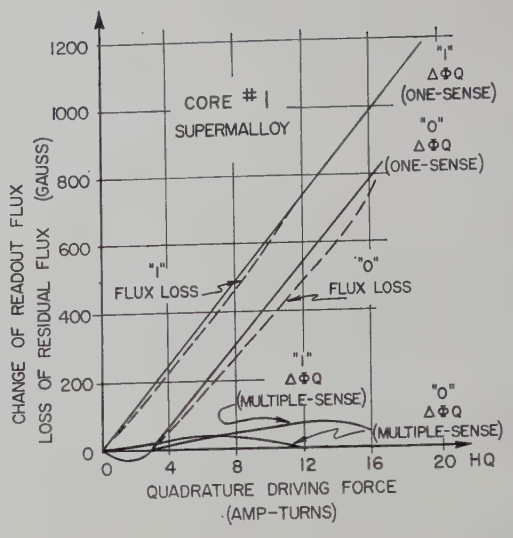
The quadrature winding can be placed either outside the conventional windings, or inside, directly against the tape surface. Reasonable care is necessary in order not to damage the tape. This fabrication does not appear sensitive to damage; and in all cases where damage was incurred, the cause apparently was due to winding the quadrature turns tightly, thus denting or stressing the tape. Lewis[7] suggested the use of a polyvinyl sleeve which is slipped over the bobbin to protect the tape during winding.

Extra wraps of permalloy were placed on the outside of the quadrature windings in an attempt to improve the efficiency of the system. The quadrature readout voltage increased about 25 per cent for three wraps of 4-79 Mo-Permalloy wrapped by hand around the core and windings. Noise voltage in the cold-worked wraps increased; therefore, this procedure does not appear attractive unless the core is manufactured with the circumferential turns sandwiched between tape layers which have retained their squareness property.

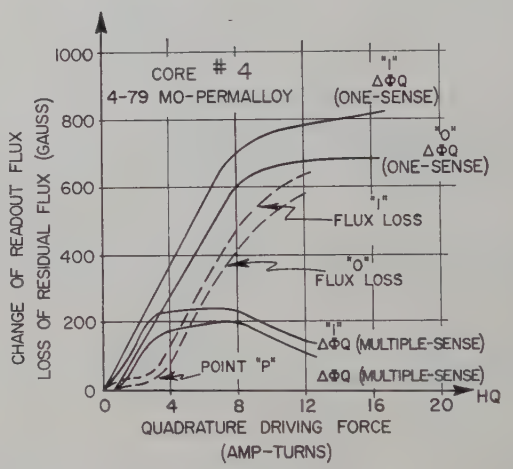
The primary requirement of any nondestructive readout system is, of course, that it be nondestructive of the remanent flux. The amount of remanent or residual flux decrease at readout is an indication of the efficiency of the particular system. Some systems, such as this quadrature field readout, are partially destructive due to the imperfect alignment of the crystals and the variation in magnitude of the magnetic moments of the domains in the polycrystalline alloy tape. Since the metallurgical properties of the alloy are paramount in quadrature field sensing, the circuit designer is interested in the relation of the quadrature field strength and the residual flux loss for the alloy tape under consideration.

Fig. 4(a)–4(c) are typical curves of this relationship. For Supermalloy, the residual flux loss approximates the flux change at all values of quadrature field. Thus, for Supermalloy, the quadrature field sensing is not nondestructive. The magnitude of residual flux for Supermalloy is about 5000 gauss. The quadrature flux change is less than 1000 gauss for the fields of interest. This means that less than 10 per cent of the total switching flux is involved in the sensing operation.

For 4-79 Mo-Permalloy, the residual flux loss abruptly increases for quadrature fields greater than about 3.2 amp-turn. The residual flux magnitude for 4-79 Mo-



(a)



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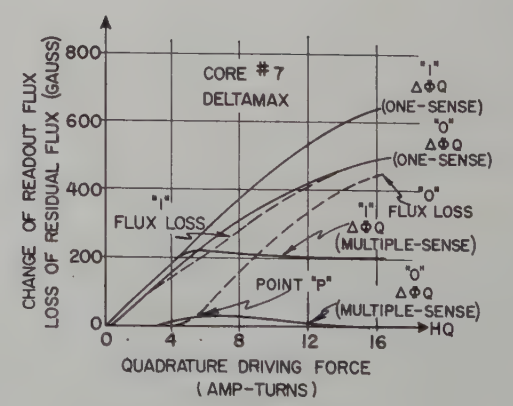

(c)

Fig. 4—Change of readout flux and loss of residual flux vs quadrature driving force. The solid lines represent the change of flux of a freshly magnetized and a multiply read core as a function of quadrature field strength. The dotted lines represent the flux loss after the first readout of the freshly magnetized core. (a) ½-mil Supermalloy. (b) ½-mil 4-79 Mo-Permalloy. (c) ½-mil Deltamax.

[7] H. A. Lewis, Arnold Engineering Co., Marengo, Ill., private communication.

Permalloy is about 5000 gauss. Maximum quadrature flux change for one-sense operation occurs at about 9 amp-turn. This field corresponds to a residual flux loss of about 500 gauss or about 10 per cent of the total switching flux of a saturation loop.

Fig. 4(c) is typical of the Deltamax cores tested. It is seen that the residual flux participating in the quadrature readout is almost entirely destructive as is the case with the Supermalloy. In addition, the Deltamax exhibits a very large dissymmetry with regard to multiple sense operation for the cores tested. Since the residual flux magnitude for Deltamax is about 14,000 gauss, only about 2 per cent of the switching flux appears to be participating in the quadrature readout.

For Supermalloy, about 50 per cent of the quadrature readout flux loss occurs during the first readout. One per cent or less occurred for each additional readout. The multiple-sense readout is the asymptotic final value of nondestroyed quadrature flux.

For 4-79 Mo-Permalloy, about 10 per cent of the quadrature readout flux loss occurs during the first readout. Subsequent readouts cause a one per cent or less flux loss per readout.

Deltamax exhibits about a 10 per cent loss of quadrature readout flux during the initial readout with a one per cent or less loss for each subsequent readout.

Experimental Shift Register

For the purposes of testing, a simple shift register was used rather than a counter or more complicated device, since the same basic problems and results are involved. Fig. 5 is a schematic diagram of the shift register which employs a standard type delay.[8] The operation of the shift register is as follows.

1) Some initial setting of the register can be made by applying a current to the input windings of the cores, Ni.

2) Shift pulses transfer the information to the capacitor of the interstage delay while the second diode D2 is back biased by the shift pulse voltage across R_{b1}, thus preventing the interstage network from discharging. The blocking voltage, generated by the noise voltage of the blocking core, back biases the first diode D1 enough to prevent noise and zero pulses from nonswitched cores from charging the interstage capacitor.

3) Upon the termination of the shift pulse, the second diode D2 is unbiased and the capacitor discharges through the input winding; Ni sets the core.

Quadrature Design Procedure

In order to design a circuit employing circumferential-turns quadrature field sensing, empirical data curves such as in Fig. 4(a)-4(c), are sufficient. An initial selection of the core material is generally determined by the particular device. For one-sense operation, the limiting value of quadrature field depends on how great a loss of flux can be tolerated. From Fig. 4(a)-4(c), the optimum quadrature field appears to be the portion of curve near the maximum curvature for minimum quadrature field (for example, 8 amp-turns for 4-79 Mo-Permalloy). For multiple-sense operation, the optimum value is at the point of the commencement of flux loss, point P in Fig. 4(b) and 4(c).

The shift register was designed using 12-wrap $\frac{1}{4}$-mil 4-79 Mo-Permalloy cores. For a 0.12-μsec current driver rise time, a value of quadrature field of about 8 amp-turns appears optimum. The flux loss at this sensing level had to be considered in the shift register design. Twenty turns were chosen for the quadrature winding. For the problem, a 2-volt output voltage was considered desirable; therefore, a 10-turn sense winding was used.

Shift Register Readout

The quadrature readout circuit shown in Fig. 6 is simply a gated collector circuit. The interrogation of the shift register occurred between shifting cycles. The flux swings involved in the interrogation did not affect the shifting operation since the loss of flux was quite small. Similarly, the shifting operation did not feed through the gated collector circuit into the output registers. This circuit was operated up to 1 mc.

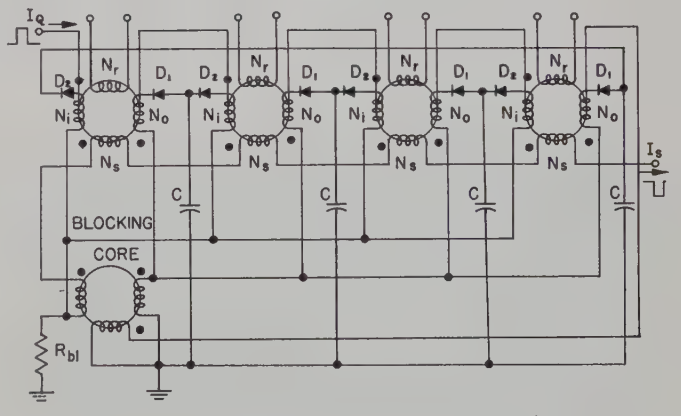

Fig. 5—Experimental shift register employing quadrature field readout.

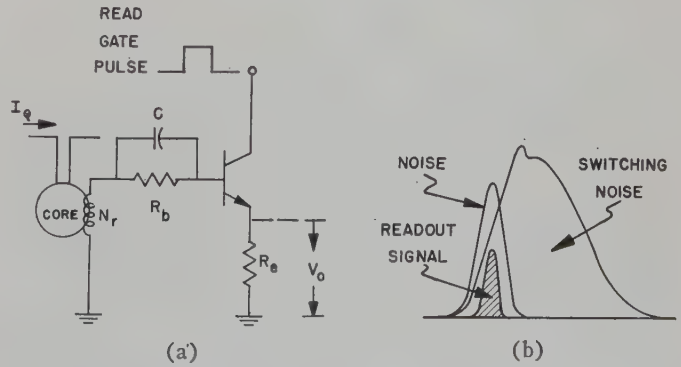

Fig. 6—Gated collector readout circuit for the elimination of noise and shifting voltages from the read output.

[8] V. L. Newhouse and N. S. Prywes, "High-speed shift registers using one core per bit," IRE Trans. on Electronic Computers, vol. EC-5, pp. 114–120; September, 1956.

Conclusions

The experimental results indicate that the circumferential-turns method of quadrature field sensing is simple to fabricate, straightforward to design, and provides useful outputs—experimentally, about 0.1-volt-per-turn output signal at about 3-ampere-turns interrogation current. The method, although not completely nondestructive, permits the designer to allow for the loss of flux since it is known for a given sensing level.

An important factor in driving the quadrature turns is that only the rise time of the pulse is important; thus, the source need only provide a rapid rise pulse and the pulse shape and duration can be of any convenient character.

Because of its nature and simplicity, the method lends itself to a variety of applications. Unless the readout pulse is stretched and amplified, it is of too short a duration to set a standard core. The readout voltage could, however, set logic gates and thus steer the core contents in accordance with the information contained in the cores. This latter aspect allows conventional core circuitry to be used and operated in the conventional manner, but with the added available feature of a built-in decision capacity. The so-called "level logic" available from current and voltage state devices is thus possible in a rather broad interpretation through the use of nondestructive readout.

Short duration and large amplitude outputs are compatible with quadrature field sensing. The sense-pulse rise time determines both quantities directly; therefore, higher operating speeds do not require a correspondingly increased drive (as with most devices), but only a faster rise in the sensing-pulse waveform.

Diode-Steered Magnetic-Core Memory*

A. MELMED† and R. SHEVLIN†

Summary—**This paper describes techniques which take advantage of word arrangement to make possible large, high-speed magnetic-core memories at moderate cost. Economy is obtained by means of a two-coordinate selection system using diffused junction rectifiers as steering diodes. By taking advantage of the relatively slow recovery time of these rectifiers, automatic rewrite selection is obtained in a similar sense to that provided by a biased switch core. The familiar "inhibit" line is eliminated, reducing the memory array to a two-wire configuration. And finally, the customary core array geometry is rearranged to facilitate winding the digit wire as a balanced twisted-pair transmission line so as to eliminate the effect of post-write disturb.**

Introduction

THIS PAPER sketches two novel techniques which, used in conjunction with the word-arranged,[1] random-access magnetic-core memory, will yield faster speeds more economically for large memory arrays. One technique exploits the property of diode hole storage to obtain automatic rewrite selection[2] in a similar sense to that provided by a biased switch core, while the other makes use of a terminated transmission line to eliminate the effect of post-write disturb. A transistorized model containing low-drive cores has been built and tested. The model exhibits an access time of 1 μsec and a cycle time of 4 μsec. Refinement of the techniques outlined here should reduce these times by a factor of 2.

First Technique

A schematic illustrating the use of germanium junction diodes for steering (selection) and automatic rewrite selection is shown in Fig. 1. Each core is threaded by three function lines, a selector line, a sense line, and an alert (in contradistinction to inhibit) line. The selector line threads all the cores of the same word, the sense and alert lines (not shown) thread cores in the same bit position of every word.

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† AEC Computing and Appl. Math. Center, Inst. Math. Sciences, New York University, New York, N. Y.

[1] "Progress on Computer Components," National Bureau of Standards, Washington, D. C.; October, 1954–March, 1955.

[2] "On the Design of a Very High Speed Computer," Digital Computer Lab., Univ. of Illinois, Urbana; October, 1951.

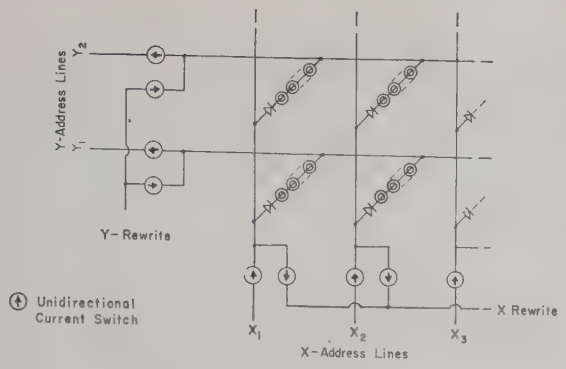


Fig. 1—Schematic drawing of diode-steered selection system for word-arranged memory.

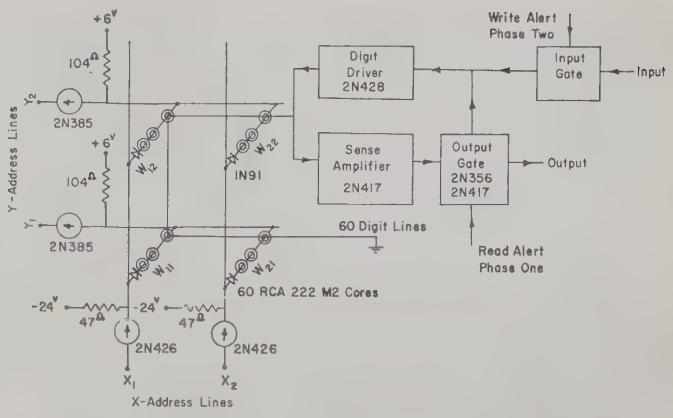


Fig. 2—Block diagram of four-word model memory.

A READ and a WRITE both consist of two sequential phases. In the first phase of a READ, one *X*-address-line and one *Y*-address-line current switch are simultaneously alerted, and supply full core switching current to the associated selector (word) line. All the cores (of the one word) threaded by that line are driven towards the "0" state, and the alerted sense amplifiers detect any signals induced on the sense windings. In the case of a WRITE, the sense amplifiers remain inhibited, and this same operation serves to ERASE the contents of the word selected; *i.e.*, it leaves all cores of that word in the "0" state. In either case, the current pulse on the selector line is of the same amplitude and time duration, and fully LOADS the base of the steering diode (a leaky bucket) with minority carriers. At the conclusion of this current pulse, the diode starts its recovery to a high value of back-resistance. In the second phase of a READ, all *X*-rewrite and *Y*-rewrite current switches are immediately alerted, but supply half-amplitude core switching current only to the selector line with the unrecovered diode, every other selector line presenting a high-impedance path by virtue of its fully recovered diode. This half-amplitude current pulse serves to half-select all cores on the tagged selector line, and simultaneously, to sweep free of minority carriers the base of the unrecovered diode, thereby restoring it to its initial, or fully recovered state, and preparing the memory for another memory cycle. The signals previously on the sense windings simultaneously control the alert line drivers so as to REWRITE only those cores previously in the "1" state. The second phase of a WRITE is identical to that just described with the difference that the alert line drivers are controlled by the contents of the new entry to the memory.

Note that "1"-state cores are always "undisturbed" in this system because of the aiding currents supplied by the alert line drivers.

Experimental Model

A block diagram is shown in Fig. 2 of an elementary experimental model conforming in all its essentials (with one exception to be discussed later) to the schematic of Fig. 1. The model consists of 4 words of core memory using RCA core type 222M2 (300 to 450 ma for full drive). The steering diodes are type 1N91; the *X*-line current switches include transistor type 2N426; and the *Y*-line, 2N385. Two transistors in parallel are used for each current switch to avoid over-dissipation for high repetition rates during testing. "Low-drive" cores are used for the same reason.

The 1N91 was selected from many candidates. Germanium junction diodes were investigated because of their generally slow recovery times *i.e.*, thick bases store large numbers of minority carriers) and the 1N91 best met the following test. Biased with a forward current of 400 ma for 1.5 μsec (the turnover time for RCA 222M2 cores at 400 ma drive being 1.8 μsec) and circuit-limited in the reverse direction at 200 ma, the 1N91 supported conduction at this amplitude for 1.5 μsec before turning off, or assuming a high value of resistance in the reverse direction. Several hundred of this diode type (1N91) were compared for this characteristic. They were all found to have substantially the same recovery time, the variation being such as not to appreciably thicken the trace on an emulsion repeatedly exposed to the same test on randomly selected samples.

In order to determine the limits of usefulness for the 1N91 in this application, it was subjected to a wider range of test conditions. The current amplitude was varied between 100 ma and 400 ma and the pulse duration between 0.2 and 1 μsec. If the recovery current was limited to half-amplitude, the recovery time remained substantially equal to the pulse duration (see Fig. 3). For pulse durations greater than several microseconds, (depending on the current amplitude) the recovery time increased more slowly than the pulse duration as internal diffusion (recovery) contributed significantly to total recovery.

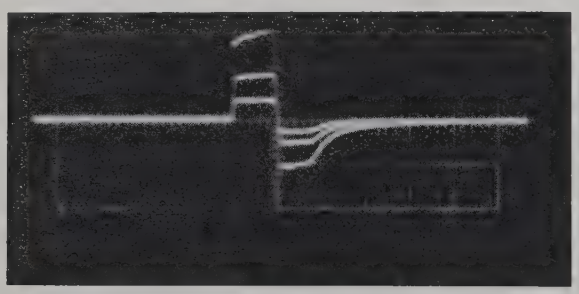
Although the authors cannot offer a satisfactory explanation at this time for these characteristics, their usefulness is not thereby diminished, and the field of applicability covers most of the core types available today.

The exception in the model alluded to earlier consists in the elimination of one of the two lines (sense and alert) threading the same bit position of each word by time-sharing their functions on a common digit line.

As previously described, the alert line functions only during phase two of a READ or WRITE, while the sense line functions only during phase one. Furthermore, the voltage induced on the sense line by the alert line current during phase two is of opposite polarity (not including post-write disturb) to the voltage induced on the sense line by a selector line current during the first phase. The voltage excursions on the digit line are therefore of opposite polarity during its two applications, and the larger phase two voltage serves only to drive into cutoff the input transistor of the connected sense amplifier.

The following is a brief description of the operation of the model. Each steering diode is back-biased by 30 volts. When, after forward conduction, it presents a low resistance to the bias voltage, the diode current is circuit limited to 200 ma. To READ the contents of word W_{11}, lines X_1 and Y_1, and the output gate for every bit position are alerted. Phase one lasts 1.5 μsec. The current distribution is shown in Fig. 4. Any core in word W_{11} switched from the "1" to the "0" state induces a positive voltage pulse on its digit line which reaches a peak in about 1 μsec. This signal is gated through the output gate to turn on the digit driver. The digit driver remains on for 2 μsec, cutting off the sense amplifier during this time. Phase two starts immediately upon the conclusion of phase one (1.5 μsec after the beginning of the READ) and lasts 1.5 μsec. The current distribution during this time for a core location which must be REWRITTEN is shown in Fig. 5.

The timing and sequence for a WRITE is almost identical, with the exception that the digit drivers are turned on only at the beginning of phase two and remain on for 1.5 μsec.



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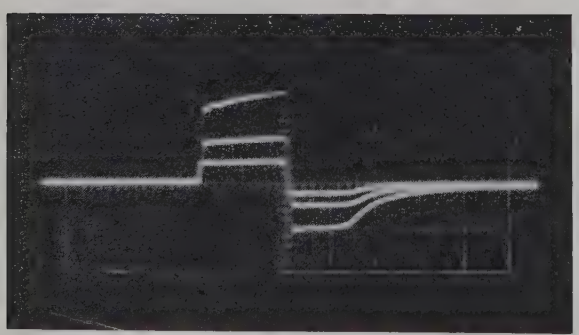

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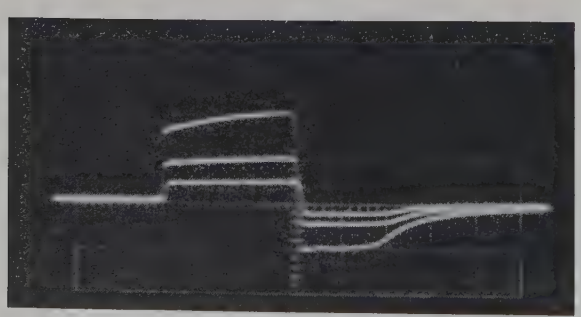


(c)

Fig. 3—Photograph of voltage waveform across 1-ohm resistor in series with diode 1N91. Diode is subjected to 100, 200, and 400 ma for (a) 0.2 μsec, (b) 0.4 μsec, and (c) 0.6 μsec, and circuit-limited to half-amplitude maximum in the reverse direction.

Experimental Results

One core of one word was continually READ and REWRITTEN at a 100-kc rate while the number of cores in the "1" state of that word was varied between 1 and 60. The current on the selector line during phase one varied between 400 and 440 ma. Under these conditions the disturbed-zero signal for RCA core 222M2 is 10 mv.

The circuitry was adjusted so that a signal of 60 mv at the input to the sense amplifier turned on the rewrite driver in the presence of a read-phase one alerting signal. This took place 0.9 μsec after the X-Y current switches were alerted (see Fig. 6).

The digit drivers remain on for 2 μsec and the post-write disturb signal extends the cycle time to about 4 μsec.

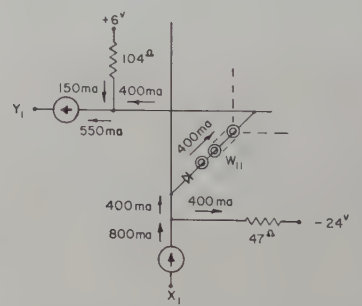


Fig. 4—Current distribution during phase one of a READ or WRITE cycle.

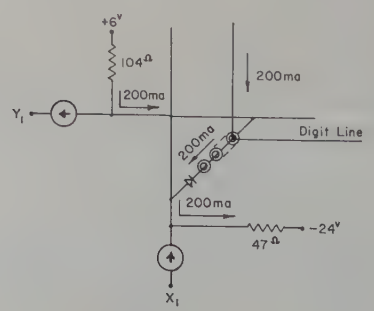


Fig. 5—Current distribution during phase two of a READ or WRITE cycle.

Second Technique

A principal factor extending the total cycle time is the post-write disturb signal on the digit line. This positive pulse (see Fig. 6) is of much greater amplitude than an "undisturbed one" and saturates the input transistor of the connected sense amplifier, prohibiting its use and extending the total cycle time (by about 1 μsec in the case cited previously).

The load on the digit line is that of the incremental permeability (virtually identical in either the "0" or "1" state) of all but one of the cores, plus the switching load presented by this remaining one, *i.e.*, a sequence of lumped inductors distributed along the length of the line. As part of a loop completed by a ground plane some distance away, this line is also susceptible to stray magnetic fields. By replacing the ground plane with a wire located adjacent to the digit line, the latter can be converted into a two-wire transmission line and terminated in its "characteristic impedance."

The half-select current pulse supplied by the digit line driver now propagates down the line at a rate determined by the line constants and is absorbed at the receiving end. This prohibits initiating a new READ or WRITE cycle for a time equal to the transmission time of the line, since the digit and selector line currents are of opposite sense (in switching a core). However, this time is much less than that of the post-write disturb. In addition, since both wires of the twisted pair are threaded through each core (as shown schematically in Fig. 7), the amplitude of the current pulse required by the digit line driver is reduced by half, and the twisted-pair transmission line is virtually impervious to stray magnetic fields.

The assembling of a core plane is accomplished by drilling out a phenolic board, of a thickness equal to the core thickness, plugging the holes with cores, temporarily sealing the cores in place with a layer of cellophane on each face, or an adhesive spray, and wiring. A partially filled phenolic board is shown in the photograph of Fig. 8 with some digit lines wired in. Fig. 9 is a close-up view of this wiring. A schematic representation of a fully wired board including the selector lines is shown in Fig. 10.

This method of assembling fixes the geometry of the array, and consequently its distributed capacity. In order to strike a balance between the "characteristic

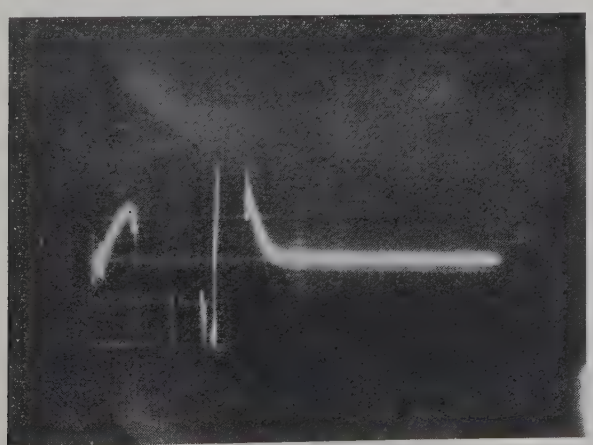


Fig. 6—Voltage waveform on a digit line during a READ cycle; vertical scale, 50 mv per division, horizontal scale, 1 μsec per division; the initial positive signal is the "undisturbed 1" input to the sense amplifier, the large negative swing following is the digit driver output voltage, and the final positive swing is the post-write disturb.

Fig. 7—Schematic illustration of digit line wiring.

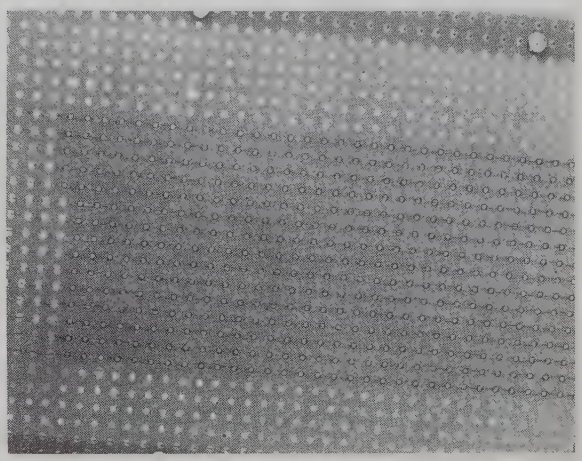


Fig. 8—Photograph of a phenolic board partially loaded (with cores) with some digit lines wired in.

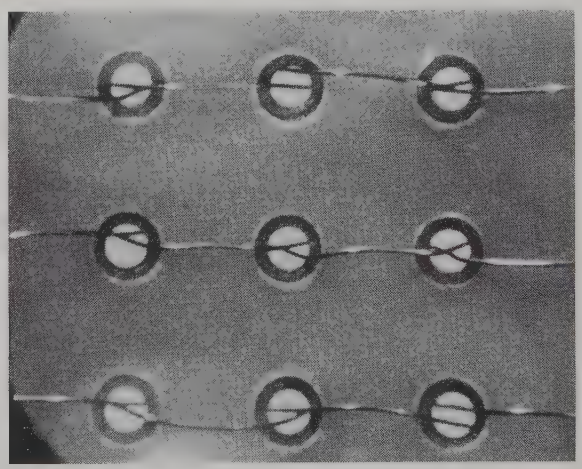


Fig. 9—Close-up view of Fig. 8.

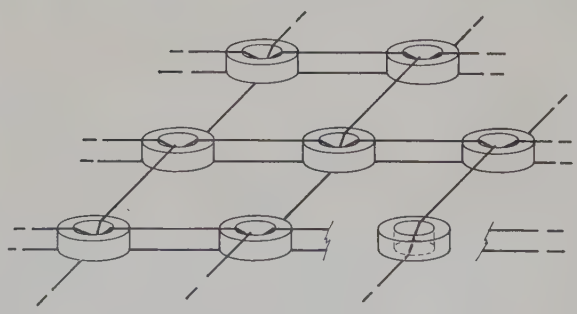


Fig. 10—Schematic illustration of selector and digit line wiring.

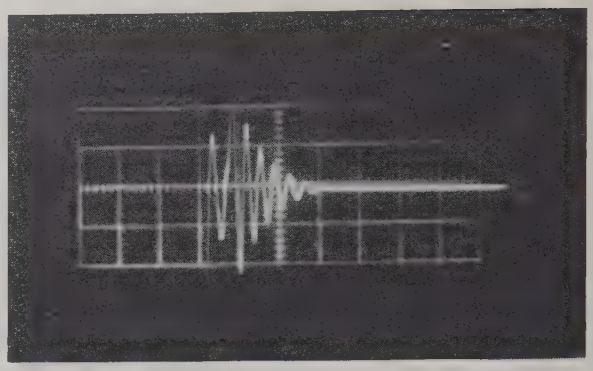
impedance" and transmission time of the line, the distributed capacity may be varied by varying the hole spacing. Using several different core types, 1000-core lines have been fabricated having transmission times between 25 and 40 mμsec, and "characteristic impedances" between 200 and 400 ohms.

The effect of this technique on ringing is shown in Fig. 11 for two 1000-core lines. Fig. 11(a) shows the voltage at the sending end of a two-wire twisted pair transmission line short-circuited at the receiving end, and driven by a current pulse of 100 ma. Fig. 11(b) shows the effect produced on the sending end voltage by terminating the line in its "characteristic impedance."

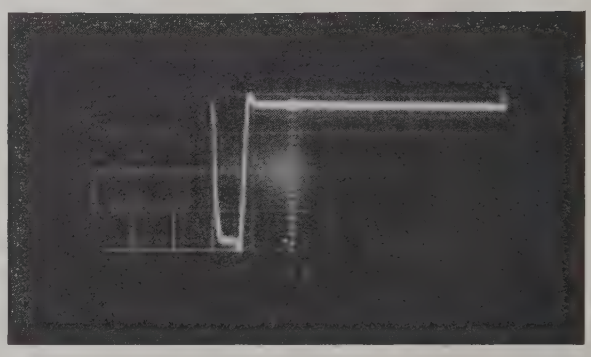
Conclusions

The results given here are only illustrative. The time necessary for phase one of a read or write cycle can be much reduced over that cited by the use of overdrive. Further, for a read cycle, it is not necessary to fully reset "1"-state cores during phase one before REWRITING them, *i.e.*, access is available well in advance of complete switching. Of course, at the completion of phase one of a write cycle, all the selected cores must be in the "0" state. The limit on the minimum time for phase two of a read or write cycle is determined here by the use of an aiding 2:1 current selection ratio, and the core type.

It should be possible, using the techniques outlined here, to build large transistorized memories at moderate costs which can be READ-REWRITTEN or ERASED-WRITTEN in 1 to 2 μsec, with an access time between 0.5 and 0.8 μsec.



(a)



(b)

Fig. 11—(a) The voltage waveform at the sending end of a two-wire twisted pair transmission line threading 1000 cores, short-circuited at the receiving end, and driven by a current pulse of 100 milliamperes; vertical scale, 5 volts per division, horizontal scale, 1 μsec per division. (b) The line has been terminated in its characteristic impedance.

Acknowledgment

The authors wish to acknowledge the contributions of R. Laupheimer, and the help of W. Landesberg and J. Marine with fabrication and measurements.

The Design of a Large Electrostatic Memory*

M. GRAHAM†, G. L. MILLER‡, H. R. PATE‡, AND R. SPINRAD‡

Summary—**A large, high-speed random-access memory for the Brookhaven "Merlin" digital computer is described. This system employs barrier grid electrostatic storage tubes in a novel configuration yielding improved reliability. Basic design considerations are presented together with a description of circuitry and performance.**

Introduction

In recent years, the trend in computer memory systems has definitely been away from the electrostatic type. Modern machines almost without exception favor some kind of magnetic memory. However, it was considered that the possibilities of the barrier grid tube had not been fully exploited and that a reliable and more economic memory could be built using these tubes.

Development of a high-speed random-access memory for Merlin, a digital computer being built at Brookhaven National Laboratory, has been carried out. Special attention was paid to an improved target reading system, less critical discrimination between "1's" and "0's," and maximum packing density of information. This memory has been built and tests have shown a performance more than adequate to meet the needs of the computer. The total system cost averages $0.10 per bit. In the discussion which follows, some familiarity with the operation of digital computer memories will be assumed.

The Radechon Tube

The system described in this report utilizes the Westinghouse WL-7565. This tube represents the most recent step in the development of the Radechon as a reliable, inexpensive digital store.

The Radechon was first reported in 1948[1] when it was viewed primarily as an analog storage device, *i.e.*, as a buffer store for TV. In 1955[2] its use in a digital system with a novel readout technique was described, and 1957 saw its first application in a large memory for a digital computer.[3] In 1958[4] the use of Radechons as a Central Office Store in telephone switching systems was described.

Each of these systems used not only different Radechons but different electronic techniques. In each case, the state of the art and the particular performance criteria dictated the mode of operation.

With the use of Figs. 1–3, we may review the Radechon's operating principles. Fig. 1 plots the secondary emission coefficient δ of a typical insulator as a function of the energy of the incident electron beam. It is seen that anywhere between 1 and 2, the first and second crossovers, more electrons will be emitted from the insulator surface than impinge upon it. The tube must be operated in this region.

Fig. 2 is a diagrammatic representation of a Radechon. The storage surface, which is an insulator, is at the right side of the figure. Directly in front of the storage surface is a barrier grid; behind it is a backplate electrode. The electron beam impinges directly (through the barrier grid) on an elemental surface area and tends to charge it to an equilibrium potential determined by the potential of the barrier grid. Fig. 3 illustrates the performance of the storage surface. It is a plot of the current I to or

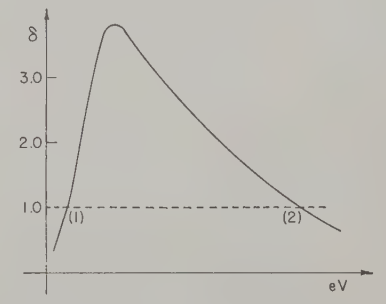


Fig. 1—Secondary emission coefficient as a function of electron energy for a typical insulator.

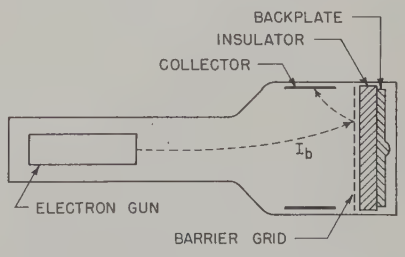


Fig. 2—Radechon storage tube.

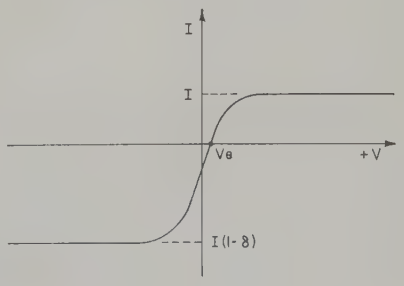


Fig. 3—Radechon target characteristics.

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[1] A. S. Jensen, J. P. Smith, H. H. Mesner, and L. E. Flory, "Barrier grid storage tube and its operation," *RCA Rev.*, vol. 9, pp. 112–135; March, 1948.

[2] M. E. Hines, M. Chruney, and J. A. McCarthy, "Radechon storage," *Bell Sys. Tech. J.*, vol. 34, p. 1241.

[3] W. Orvedahl, private communication.

[4] T. S. Greenwood and R. E. Staehler, "A high-speed barrier grid store," *Bell Sys. Tech. J.*, vol. 37, p. 1195; September, 1958.

from the surface as a function of the surface potential V relative to the potential of the barrier grid. Ve, which is normally one or two volts positive, is the equilibrium potential relative to the barrier grid. In the system we are describing, the barrier grid is maintained at ground potential so that, for this case, V also represents the absolute potential.

The tube stores information in the form of a charge pattern on the surface of the insulator. To WRITE on an elemental area, the backplate potential is first changed by a certain amount. This change is capacitatively coupled to the front surface of the insulator where it produces a change, ΔV, from the equilibrium potential. At this point the potential of all the elemental areas have been changed by ΔV. Next, the selected area is bombarded by the electron beam. This causes the spot to charge back to the equilibrium potential Ve, *i.e.*, to experience a change of potential ΔV. The beam is then turned off and the backplate returned to its original potential. All the unselected areas return to their starting potential. The selected element is, however, charged to $-\Delta V$.

In order to READ the stored information the beam is directed at the selected spot without changing the backplate potential. The resulting charge or discharge current is a measure of the stored information. Jensen, *et al.*[1] described the use of this tube as an analog device. In this application the upper limit to ΔV was set by the extent of the linear region of the plot of Fig. 3. The charge or discharge current was then directly proportional to original applied voltage. Since writing was to be done rapidly, the applied ΔV was always negative. This took advantage of the increase in writing rate afforded by the $(\delta-1)$ multiplication of the beam current.

In the remainder of the referenced systems the storage was digital. This removed the restriction on the extent of ΔV, since there was no need for fine gradations in the READ current. In fact, ΔV was in all cases made considerably larger than the linear region.

The digital systems described were all binary and recognized the two stored potentials, Ve and $(Ve+\Delta V)$. The concept of bidirectional operation, although alluded to,[2] had not been explored until one of the authors (Graham) pointed out its advantages. In this system the two information potentials are $(Ve+\Delta V)$ and $(Ve-\Delta V)$. The equilibrium potential Ve is disallowed. The chief advantage is that the READ currents are distinctly bipolar. This technique, coupled with that of target reading, facilitates discrimination in the presence of noise and circuit drift.

The sensing of the READ currents can be done at two places: the target and the collector. The systems described previously[1,3,4] detected at the collector, whereas Hines, *et al.*[2] described target detection. Collector detection involves discrimination between unidirectional current pulses of different magnitudes, and target reading involves discrimination between the absence or presence of a pulse[3] or, in our case, between pulses of opposite polarity.

Clearly, target reading should be chosen if one serious drawback can be eliminated. This limitation is that the WRITE signals applied to the backplate are of the order 10^5 times the READ signals to be detected at the same location. This presents serious overload problems to the READ amplifier, especially if recovery time is a consideration. Curiously, while the solution to the problem was developed by Bell Laboratories,[2] it was not pursued by them.[4] This solution treats the entire target structure, *i.e.*, the backplate, insulator, and barrier grid, as the element to which the READ signal flows (see Fig. 4). The packplate WRITE signal was applied through a coaxial cable wound as a coil. The charging WRITE current through the center of the cable is cancelled by the return current flowing through the braid. If the cancellation were perfect, no signal would appear at the READ electrode. The READ current, on the other hand, does produce a signal across the coil inductance. The perfection of this technique is of paramount importance to the development of this system and is discussed more fully in another section of this paper.

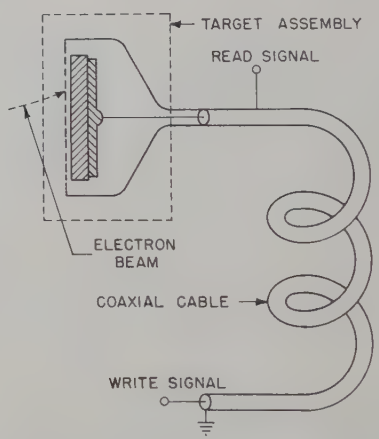

Fig. 4—Bell Laboratories target reading system.

The development of the WL-7565 was undertaken by Westinghouse in conjunction with Brookhaven National Laboratory. The object was to produce a Radechon of high quality with features consistent with the requirements of the system described here.

The WL-7565 has a coaxial target structure to facilitate target reading. The insulator used is mica. In order to provide the same WRITE and READ currents for both polarities it is desirable to operate the target at a secondary emission ratio of two. Mica has this ratio at approximately 1.2 kv. The secondary emission of the barrier grid (which produces a spurious signal if other than one) is rigidly controlled. The storage surface uniformity is carefully monitored because variations in its secondary emission ratio also introduce spurious signals. The tube has a large target area and does not require dynamic focusing.

Logical Design

Each tube has associated with it the circuitry shown in block form in Fig. 5. The operation can best be seen by referring to the timing chart in Fig. 6 (the shaded areas in that figure are the times for which the beam is on). Suppose that the beam has just been switched on for a READ; simultaneously, the READ gate opens. If the signal is negative (indicating a "1") and exceeds a certain value, it will trip the trigger circuit at some time during the strobed interval. If, however, the READ signal is positive, it cannot fire the trigger circuit. Now, since it will be seen from Figs. 5 and 6 that the flip-flop is always in the zero state just before the beam goes on (because of the WRITE 0 at the end of the previous BEAM-OFF pulse), the state of the flip-flop when the READ gate closes represents the information that was stored at the location that has just been read. The application of the WRITE TRIGGER PULSE then fires the appropriate "1" or "0" blocking oscillator, the output of which drives the backplate positive or negative, leading to the REWRITE operation. At the end of the REWRITE the beam goes off, the backplate is returned to ground ready for the next READ, and the flip-flop is reset to "0." This completes a regeneration. A FETCH is identical except that the output of the "1" blocking oscillator is gated out to the machine, with a pulse signifying a "1" and the absence of a pulse a "0."

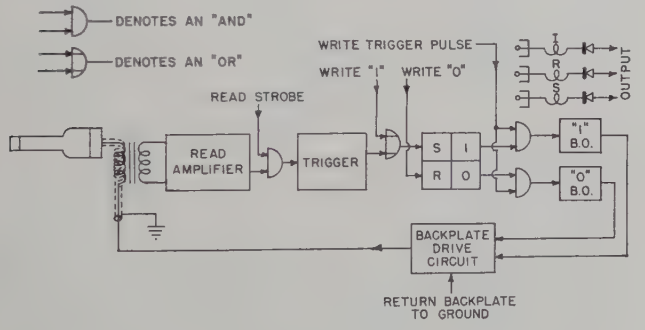

Fig. 5—Logic associated with each tube.

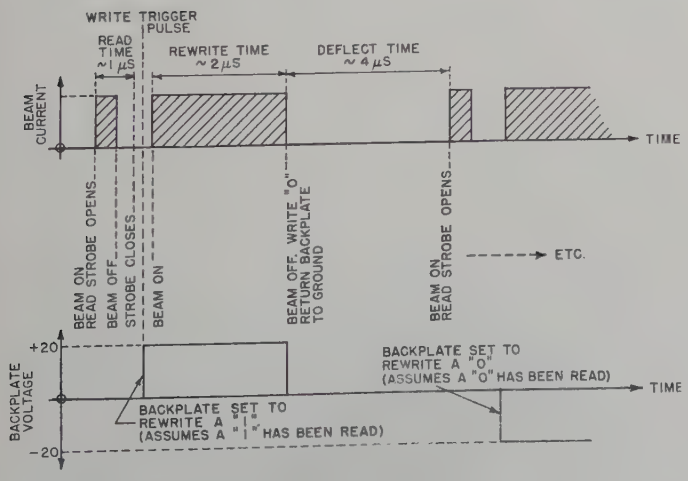

Fig. 6—Timing cycle.

A STORE operation is an obvious variation of the process that has just been described. The flip-flop is set to the desired state and, as a result, the backplate is switched in the appropriate direction by the action of the WRITE trigger pulse just as before. The only feature that is different is that the beam is now switched ON and OFF only once instead of twice as in the previous operation, and the READ strobe is kept closed. The BEAM-ON period for writing is also independently adjustable.

It is the purpose of this paper to describe only the system shown in Fig. 5 and its performance under test conditions. No further discussion will be given of the total system, which comprises 196 such units.

Target Reading System

Initial attempts at Brookhaven to utilize the Bell Laboratories target reading system were far from successful, since large breakthrough signals were obtained. A simple analysis of the input circuit revealed the source of the difficulty, and indicated how to achieve good cancellation. This treatment can be understood with the help of Fig. 7 where the "inner" and "braid" windings of the primary have been separately exposed. (The use of a separate signal winding to drive the READ amplifier is a matter of convenience and does not affect the argument.) In this diagram the components have the following significance.

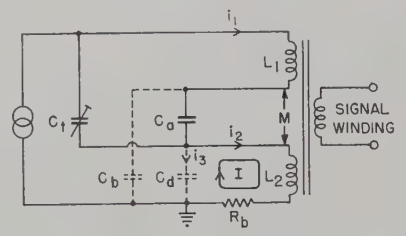

Fig. 7—Target reading equivalent circuit.

C_a = backplate to barrier grid capacitance.
C_b = backplate to ground capacitance.
C_d = barrier grid to ground capacitance.
C_t = trimmer capacity.
R_b = resistance of the braid of the coaxial cable.
L_1, L_2 = inductance of the inner and braid windings, respectively, on the transformer. These are clearly almost exactly equal, so it is allowable to set $L_1 = L_2 = L$.
M = mutual inductance between L_1 and L_2.

It has already been remarked that the object of the design is to insure that upon switching the backplate, equal and opposite currents flow in the inner and braid of the primary. The BREAKTHROUGH signal is a consequence of the currents that flow in the stray capacitances C_b and C_d. The former can be minimized by completely enclosing the backplate in a continuation of the barrier grid and then employing a trimmer C_t to

"replace" the remainder of the current that flows through C_b.

The way to minimize the effect of C_e can be seen by writing the equation for loop I in the form

$$\frac{\int i_3 dt}{C_d} = R_b i_2 + L\frac{di_2}{dt} - M\frac{di_1}{dt}.$$

Then, if C_t has been correctly adjusted,

$$i_1 \cong i_2 + i_3.$$

Hence,

$$\frac{\int i_3 dt}{C_d} + M\frac{di_3}{dt} = R_b i_2 + (L - M)\frac{di_2}{dt},$$

from which it is clear that if $R_b = L - M = 0$, the LHS would be identically "0"; hence, both the derivative and integral of i_3 would individually be "0," and, consequently, i_3 would be zero. Therefore, to minimize the effect of C_d, the primaries should have the tightest possible coupling, and the coaxial cable should have low braid resistance.

The four conditions for a small BREAKTHROUGH signal can therefore be summarized as follows.

1) Enclose the backplate. } Minimizes the
2) Employ a bucking signal. } effect of C_b.
3) Use closest possible coupling between the two primary windings. } Minimizes the
4) Use coaxial cable having the lowest possible braid resistance. } effect of C_d.

In the Merlin memory, these conditions are fulfilled by using specially designed input transformers, details of which are given in Fig. 8, and a Radechon with an enclosed backplate. As a result the BREAKTHROUGH signal is considerably smaller than the READ signal itself, indicating a balance of better than 1 in 10^5 in the input circuitry. Photographs of the backplate, READ and BREAKTHROUGH waveforms are shown in Fig. 14.

READ Gate and Trigger Circuit

An element was required which would accept the output from the READ amplifier, discriminate against noise and other extraneous signals, and produce a sharp pulse upon receipt of a "1" signal. It was then necessary to produce a triggering pulse at the correct time to fire the "1" or "0" blocking oscillator, as required. It was found convenient to use transistor techniques for the READ gate and trigger circuit, the schematic of which is shown in Fig. 9. As a safety precaution, diodes were connected where possible between the base of each transistor and ground to prevent excessive positive voltage excursion at these points.

The signal from the amplifier is connected to the READ gate transistor. The READ gate consists of a surface barrier transistor type 2N344 with its emitter-collector impedance connected across the signal path. Normally, a negative bias is applied to its base so that the emitter-collector resistance is very low and the signal path is short-circuited. At the same time, as the Radechon beam is switched on to READ, the base of the READ gate transistor is pulsed slightly positive with respect to ground for long enough to allow a possible "1" signal to reach full amplitude. Under this condition the READ gate transistor emitter-collector path is high resistance, and any signal output can pass to the trigger.

The trigger consists of two transistors (2N393) connected as a univibrator having a pulse time of about 1 μsec. The triggering level is adjusted by means of a potentiometer. This form of circuit was chosen since the threshold stability is excellent and gives a sharp output pulse independent of the magnitude and shape of the triggering pulse.

The output pulse from the univibrator caused by a "1" signal is passed to two further transistors (2N247) connected as a flip-flop having a collector excursion from −20 V to ground. A negative pulse is applied to the reset lead at the end of each READ-WRITE cycle, so that at the beginning of the next cycle the flip-flop is always in the "0" position. Hence, unless a pulse is received from the univibrator indicating a "1," a "0" condition is maintained. Connected to the two collectors are windings of a transformer which is pulsed from a common source at the correct time. As a result, the blocking oscillator trigger lead which is returned to the collector standing at ground has a +15 volt pulse applied to it. This is sufficient to overcome the bias of the blocking oscillator and "fire" it. The other trigger lead being returned to −20 volts prevents the +15 volt pulse from being effective.

Consequently a "1" signal at the input, or a "WRITE 1" signal applied to the flip-flop, causes the "1" blocking oscillator to fire at the correct time in the cycle; absence of either of these conditions causes the "0" blocking oscillator to be triggered. These in turn switch the backplate of the Radechon tube to a positive or negative potential. An explanation of this part of the circuit is given in the next section.

Backplate Driver

As can be seen from the block diagram of Fig. 5, at the completion of a READ operation the referenced storage location must be "rewritten." This is done by changing the potential of the backplate (and hence the storage surface) to either a positive or negative potential, and then turning on the beam. The beam reestablishes the equilibrium potential (within a volt of ground) at the selected location. When the beam is turned off and the backplate returned to ground, the selected spot is charged to a potential of opposite sign compared to the original backplate excursion. Thus, if the backplate were originally driven negative the stored spot would exhibit a positive charge, and vice-versa.

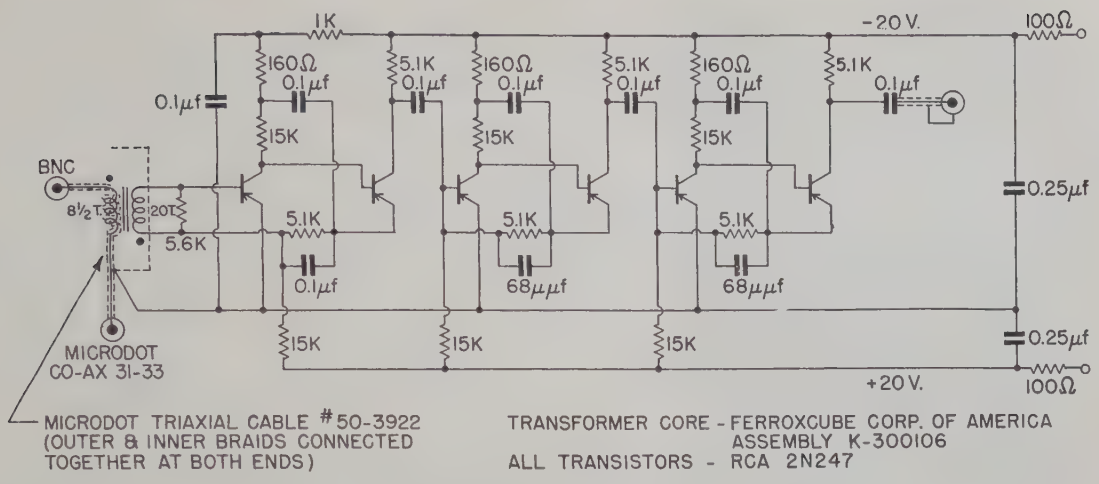

Fig. 8—READ amplifier.

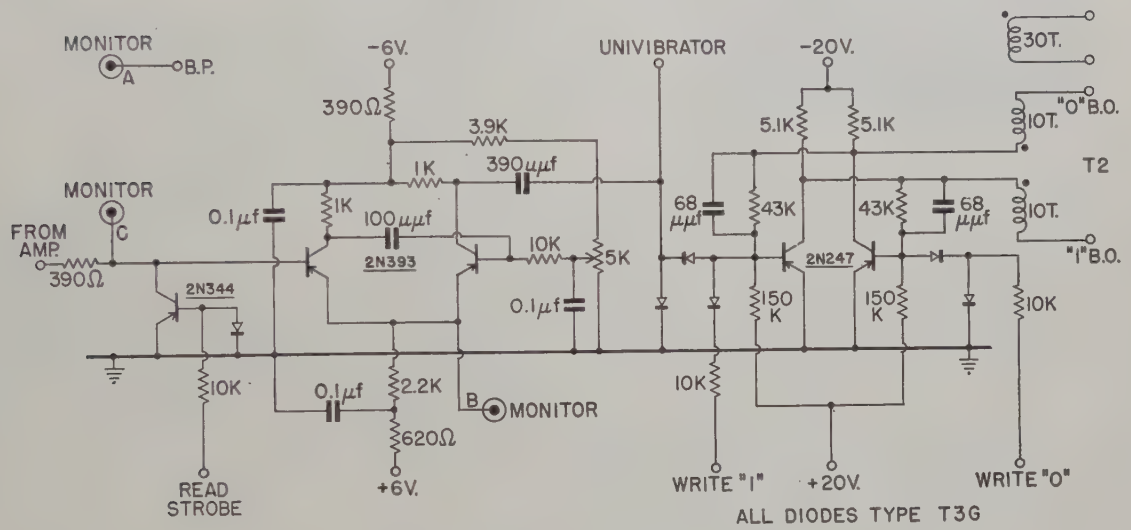

Fig. 9—READ gate and trigger circuit.

The backplate is also driven to perform a WRITE. This is the action of storing either a "1" or a "0" (a negative or positive charge) regardless of what was previously there. This is done when new information is to be stored in the memory.

Clearly then, what is needed is a circuit which quickly and reliably sets the backplate to a fixed positive or negative potential in response to one or another input signal. Also needed is a circuit which restores the backplate to "0" potential at the completion of the RE-WRITE or OVERWRITE operation. Illustrated in Fig. 10 is a diagram of the circuitry used to obtain these results.

In the figure the various pulse generators have the following functions.

SN—set backplate to a negative potential.
SP—set backplate to a positive potential.
RN—reset backplate from a negative potential.
RP—reset backplate from a positive potential.

C_{bp} represents the backplate capacity. Examination of the circuit will reveal that due to the action of the crystal diodes, in the absence of a pulse from any of the

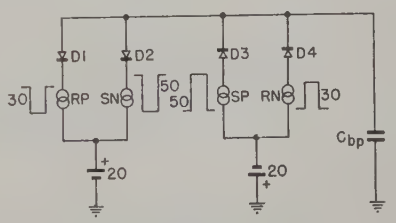

Fig. 10—Backplate driver logic.

pulse generators, the backplate will be maintained at any given voltage between ±20 volts. In particular, if the backplate were at ground potential, it would remain there. This is considered the normal state.

Consider what takes place upon the imposition of the *SP* pulse. The 50-volt positive pulse originates from a −20-volt level. This causes diode D3 to conduct and charge C_{bp} to +20 volts; it is clamped at the +20 V bus. When the pulse terminates, C_{bp} remains charged 20 volts positive because all the diodes are back-biased.

A similar operation takes place when *SN* is applied. At the completion of this pulse, C_{bp} is left charged to −20 volts.

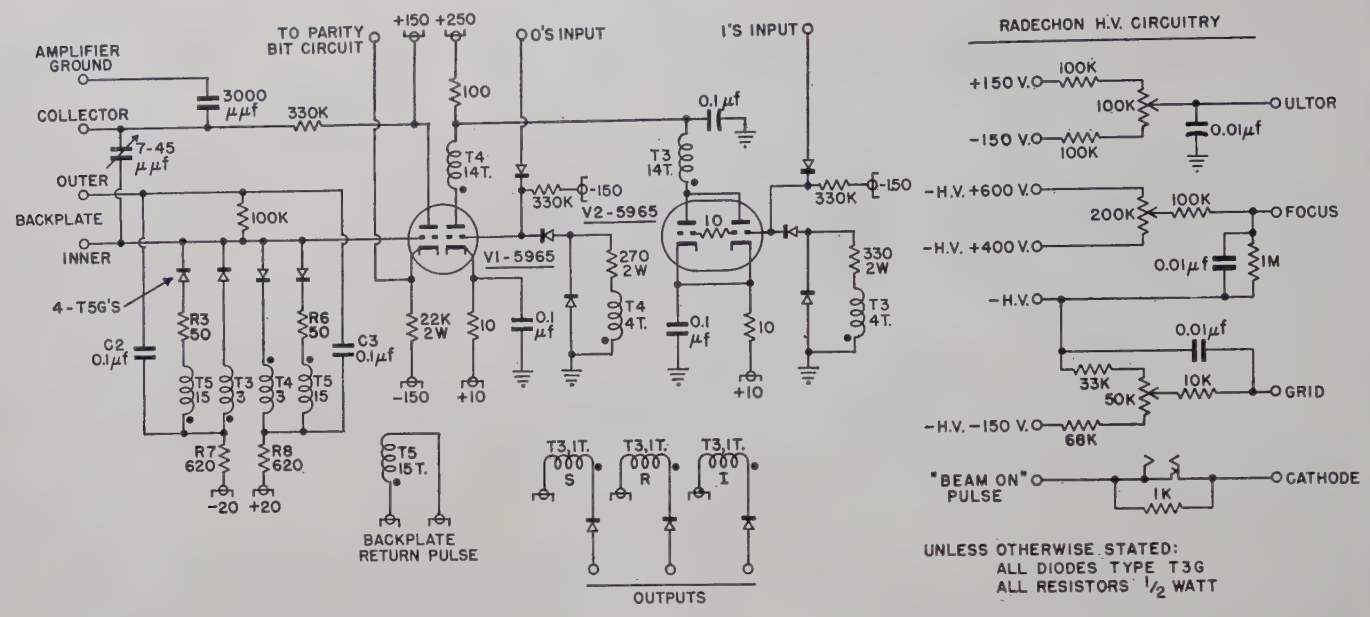

Fig. 11—Blocking oscillator and backplate driver schematic.

When it is desired to return the backplate to 0 volts, *RP* and *RN* are applied simultaneously. *RN* tries to set the backplate to +10 volts; *RP* attempts to force it to −10 volts. Since they are driven from the same generator and have equal output impedances (which are greater than those of the diodes), the final potential to which C_{bp} is forced is 0 volts.

Refer now to Fig. 11, which is the actual schematic diagram of the backplate drive circuitry. The blocking oscillator using both sides of *V2* is the pulse generator *SP*. That using the right side of *V1* is the pulse generator *SN*. *RP* and *RN* are seen to be two secondary windings on transformer *T5*, which is driven externally. The resistors *R7* and *R8*, and the capacitors *C2* and *C3*, are decoupling elements.

The variable capacitor *C1* is used to provide a correction signal for one of the components of the spurious BREAKTHROUGH, which was discussed in the section on target reading.

The blocking oscillator using tube *V2* also serves to read out the information to the rest of the system. The three windings, *S*, *R*, and *I*, provide for the transfer from memory to three different portions of the computer. This circuit uses a dual triode to enable it to satisfactorily accommodate the extra load.

(The left side of *V1* is a cathode follower used to monitor the state of the backplate for the parity check circuitry, which will be discussed elsewhere.)

In the design of this part of the system, considerable attention was given to the possibility of continuing the use of transistors. Two possibilities were examined and then, unfortunately, had to be dismissed because suitable high-speed, high-voltage transistors were not then available.

Physical Arrangement

Physically, the backplate drive circuitry is arranged on a printed circuit board. On this same board are located the Radechon's high-voltage circuitry. As can be seen from Fig. 12, this configuration provides ease of wiring and economy of lead length. For leads which are common to all four of the memory drawer Radechon circuits, terminals are soldered directly to the printed board and then cross-wired to the common bus. In those places where there is a multiplicity of cross connections, as in the high voltage circuitry, communication is provided by a "telephone pole" type of structure which can be seen in the upper right of Fig. 12. Fig. 13 shows the Westinghouse Radechon with its associated READ amplifier.

Experimental Results

The raster employed consists of 8192 storage locations arranged in the form of 32 blocks of 256, with the spacing of one spot from its neighbor's approximately 18 mils. The readaround test is made by writing an interlaced pattern of "1's" and "0's" on alternate lines of the raster; the pattern of 4096 "1's" is then regenerated without regenerating the "0's." The number of cycles before a zero failure occurs is proportional to the readaround ratio. The lowest readaround figure obtained on this test is 800 for the poorest tube. The majority of tubes exhibit readarounds in excess of 1000.

Rather extensive tests have shown that the tubes are simple to set up initially. The procedure employed is to adjust the beam current until the "1" signal at the monitor point *C* of Fig. 9 is 2 volts (corresponding to ~1 μa of beam current). The focus and astigmatism are then adjusted until the envelope of the 4096 "1's" seen

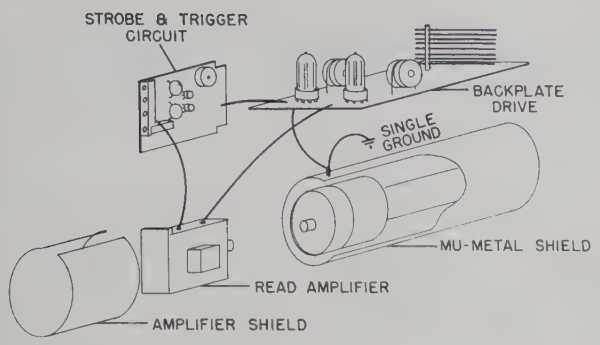

Fig. 12—Exploded view of circuit elements associated with one tube.

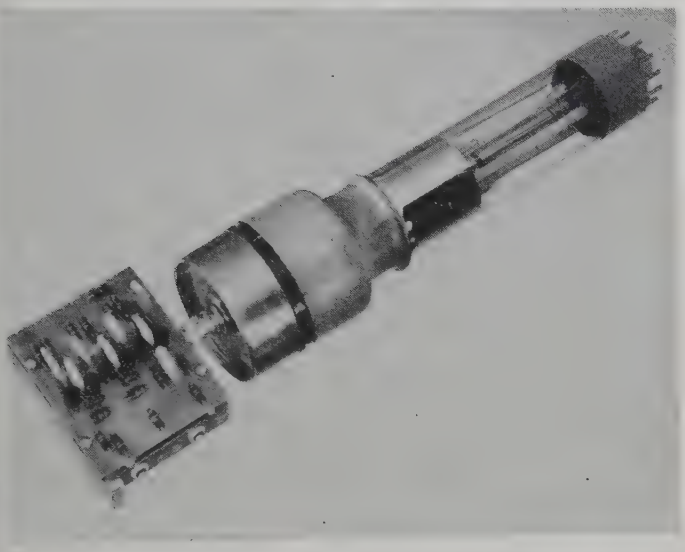

Fig. 13—Radechon tube and READ amplifier.

at the monitor point exhibits greatest raggedness. (This means that the spot is well focused and therefore reveals surface nonuniformities most markedly.) The maximum to minimum "1's" signals vary by less than 50 per cent and it is found that half a volt of discriminator bias represents about the optimum bias setting (though this value is not critical).

Fig. 14 shows the waveform associated with this type of test. In all cases the time scale is such that one large division represents 1 μsec. All traces are in their correct time relation.

Fig. 14(a) is the READ strobe signal (see also Figs. 5, 6 and 9). The leading edge of this signal also marks the time that the Radechon beam is turned on. The noise in the strobe interval, observed at monitor point *C* of Fig. 9, in the absence of any signal (obtained by switching off the high-voltage supply to the Radechon tubes) is shown in Fig. 14(b). This trace is to be compared with

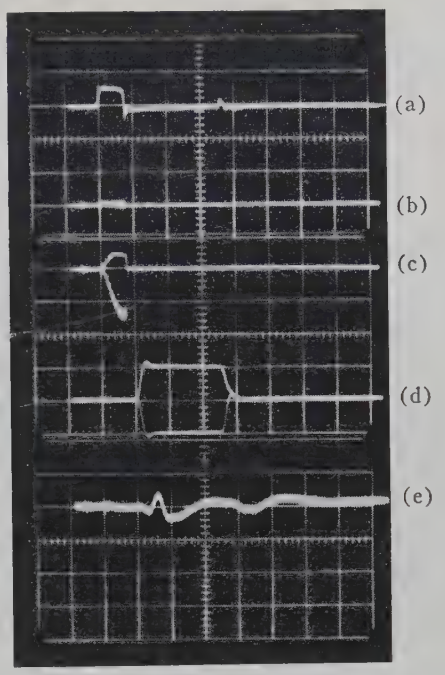

Fig. 14—Radechon reading and backplate waveforms.

the READ signal from 8192 random "1's" and "0's" shown in Fig. 14(c). Here the negative peaks are the superimposed "1's" and the positive peaks, the "0's." The latter are clamped at +0.4 volts for reasons that will be clear from an inspection of the strobe circuit of Fig. 9. The vertical scale in all three of these traces is 1.0 volt per large division.

The ± 20 volt backplate signal is shown in Fig. 14(d), while the BREAKTHROUGH signal resulting from signals of one polarity is given in Fig. 14(c). In this last trace the scale is again 1.0 volt per large division, and it is clear that this signal is smaller than the READ signal. This last trace, incidentally, was obtained by leaving the strobe permanently open and pulsing the backplate in one direction only. In practice, of course, even this small BREAKTHROUGH signal never reaches the trigger circuit because the READ gate is closed.

Acknowledgment

It is a pleasure to thank J. B. H. Kuper, W. A. Higinbotham, and R. L. Chase of Brookhaven National Laboratory, J. Richardson of Los Alamos Scientific Laboratory, and W. Orvedahl of the University of Chicago for innumerable helpful discussions. We would also like to record our appreciation for the cooperation of A. S. Jensen and R. Stow of Westinghouse Electric Corp., and D. Harsh of RCA. Our thanks are also due to L. Davis for his work on the construction of the system.

Systematic Scaling for Digital Differential Analyzers*

ARTHUR GILL†

Summary—The usefulness of large-capacity digital differential analyzers (DDA's) is severely hampered by the complexity of the scaling process. The scales needed for programming a DDA have to be compatible with the so-called "equilibrium," "topological," and "boundary" constraints, imposed by the construction of the analyzer and the nature of the problem at hand. Simultaneous trial-and-error satisfaction of all these constraints, to achieve optimal range and accuracy of computation, is practically impossible for any problem involving more than a few integrators. The paper shows how the scaling constraints can be organized in a matrix form, and how optimal scales can be produced in a systematic manner. The proposed scheme, which can be programmed for automatic execution, is adaptable for DDA's operating in conjunction with general-purpose digital computers.

Introduction

FROM a functional standpoint, a digital differential analyzer (DDA) consists of packages, each containing an integrator and an associated constant multiplier. The integrator receives incremental inputs of two different types, called the *dy* and *dx* inputs. The *dy* inputs are accumulated in a register to form the integrand *y*. The increments *dx* of the variable of integration *x* control the addition (or subtraction) of *y* into another register, called the *r* register. Overflows of *r* are increments of the integral of *y* with respect to *x* and can be accumulated in another integrator. The integral of *y* with respect to *x* is called *z*, and the increments of *z* are called *dz*. The *dz* outputs of each integrator control the addition (or subtraction) of a constant *k* into a register called the k_r register. Overflows of k_r are called *kdz* outputs of the integrator, and can serve as inputs (*dx*, *dy* or both) to other integrators. The *kdz* outputs represent increments of the integral of *ky* with respect to *x*. An integrator may have only one *dx* input, but as many *dy* inputs as permitted by the capacity of the *dy* accumulators. Fig. 1 is a schematic representation of an integrating package in a DDA.

Integrating packages of the type described above can be interconnected to provide digital solutions to differential or algebraic equations—linear or nonlinear, single or simultaneous. Fig. 2 shows, as an example, an interconnection of integrators to provide the solution to

$$\frac{d^2y}{dt^2} + \frac{dy}{dt} - y^2 - \sin y = 0.$$

The solution is registered in integrator no. 3 and can be typed out periodically during computation.

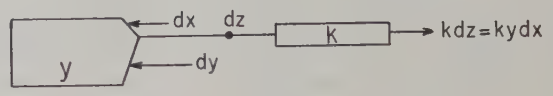

Fig. 1—An integrating package.

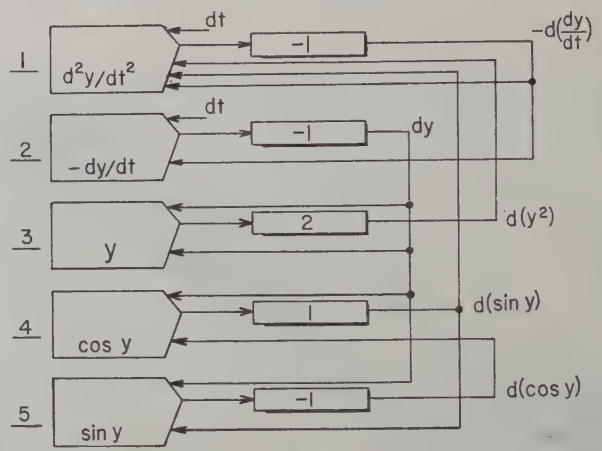

Fig. 2—Integrator network for

$$\frac{d^2y}{dt^2} + \frac{dy}{dt} - y^2 - \sin y = 0.$$

Further details concerning the construction and programming of DDA's can be found in the references.[1–3]

DDA Scaling

In a digital differential analyzer the quantities *y*, *k*, *dx*, *dy*, and *dz* are manipulated under the fixed-point system. The position of each quantity with respect to the binary point in the register is dictated by a "scale" associated with that quantity. Specifically, this scale equals the power of 2 by which the register quantity has to be multiplied in order to yield the true value. In the following discussion α_i, β_i, γ_i, δ_i, and ϵ_i will denote the scales associated with the *y*, *k*, *dx*, *dy* and *kdz* quantities, respectively, in the *i*th integrating package.

If there are *N* packages in a given problem, $5N+1$ scales have to be specified by the programmer, *i.e.*, 5 scales for each participating package, plus a scale denoted ϵ_0 for the independent variable. These scales cannot be specified independently. First, for each integrating package the following "equilibrium constraint" has to be satisfied:

$$\alpha_i + \beta_i + \gamma_i = \epsilon_i \qquad i = 1, 2, \cdots, N. \tag{1}$$

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[1] G. F. Forbes, "Digital Differential Analyzers," G. F. Forbes Publication, Pacoima, Calif ; 1956.

[2] M. Palevsky, "The design of the Bendix digital differential analyzer," PROC. IRE, vol. 41, pp. 1352–1356; October, 1953.

[3] "Programming Manual for the DA-1—Digital Differential Analyzer Accessory for the Bendix G-15D Computer," Bendix Computer Div. of Bendix Aviation Corp., Los Angeles, Calif.; 1957.

Second, the interconnection diagram implies "topological constraints" of three types: 1) Since every *dx* input is a *kdz* output, every γ_i has to be equal to some $\epsilon_j (i \neq j)$. 2) Since every *dy* input is a *kdz* output, every δ_i has to be equal to some ϵ_j. 3) If the *kdz* outputs of integrators $a, b, \cdots, g$ all serve as *dy* inputs to the same integrator, then $\epsilon_a = \epsilon_b = \cdots = \epsilon_g$.

In order to realize the highest computational accuracy, it is necessary to choose α and β scales such that the corresponding registers will accumulate the largest possible number of significant digits without overflowing during the problem run. Scales for which the above condition is realized will be called "optimal scales." Letting $\hat{y}_i$ be the maximum value that the ith integrand assumes in a given problem, the optimal α and β scales are then given by:

$$\alpha_i = \{\log_2 \hat{y}_i\} \tag{2}$$

$$\beta_i = \{\log_2 k\} \tag{3}$$

where $\{a\}$ denotes the smallest integer which equals or exceeds a.

Determining a set of scales compatible with the equilibrium and topological constraints, and at the same time realizing optimal operation, is seen to be quite involved when the problem at hand requires more than 10 or 15 integrators. Establishing the scales by trial-and-error methods is tedious at best, and often unfeasible.

In the following sections a procedure will be described by which scales can be produced in a systematic manner, possibly with the aid of a digital computer.

Matrix Formulation of the Scaling Constraints

Considering the example described by Fig. 2, the equilibrium constraints can be written as

$$\alpha_i + \beta_i + \gamma_i = \epsilon_i \qquad i = 1, 2, \cdots, 5. \tag{4}$$

The topological constraints of type 1) are

$$\gamma_1 = \epsilon_0, \quad \gamma_2 = \epsilon_0, \quad \gamma_3 = \epsilon_2, \quad \gamma_4 = \epsilon_2, \quad \gamma_5 = \epsilon_2; \tag{5}$$

of type 2) they are

$$\delta_1 = \epsilon_1, \quad \delta_2 = \epsilon_1, \quad \delta_3 = \epsilon_2, \quad \delta_4 = \epsilon_5, \quad \delta_5 = \epsilon_4; \tag{6}$$

and of type 3) they are

$$\epsilon_1 = \epsilon_3 = \epsilon_4. \tag{7}$$

Substituting (7) in (5) and then eliminating the γ's from (4), yields

$$\left.\begin{aligned} \alpha_1 + \beta_1 + \epsilon_0 - \epsilon_1 &= 0 \\ \alpha_2 + \beta_2 + \epsilon_0 - \epsilon_2 &= 0 \\ \alpha_3 + \beta_3 + \epsilon_2 - \epsilon_1 &= 0 \\ \alpha_4 + \beta_4 + \epsilon_2 - \epsilon_1 &= 0 \\ \alpha_5 + \beta_5 + \epsilon_2 - \epsilon_5 &= 0 \end{aligned}\right\}. \tag{8}$$

The above steps can be carried out in any given problem to yield a set of equations of the form

$$\alpha_i + \beta_i + \epsilon_j - \epsilon_k = 0. \tag{9}$$

The number $M+1$ of different ϵ's appearing in (9) is smaller than $N+1$ for all problems in which there is at least one integrator having more than a single *dy* input. Since this is the case in all problems involving addition (or subtraction), and hence in all nontrivial problems, it will be invariably assumed that $M<N$. By noting that ϵ_0 always has to appear in (9), and that the numbering of the integrating packages can be chosen arbitrarily, it can be assumed without loss of generality that the ϵ's appearing in (9) are $\epsilon_0, \epsilon_1, \cdots, \epsilon_M$. Using this assumption, the coefficient matrix for (9) can be written as shown in (10).

$$\begin{array}{c} \\ 1 \\ 2 \\ \cdot \\ \cdot \\ N \end{array} \begin{array}{c} \begin{array}{cccccccccccccc} \alpha_1 & \alpha_2 & \cdot & \cdot & \alpha_N & \beta_1 & \beta_2 & \cdot & \cdot & \beta_N & \epsilon_0 & \epsilon_1 & \cdot & \epsilon_M \end{array} \\ \left[\begin{array}{cccccccccccccc} 1 & 0 & \cdot & \cdot & 0 & 1 & 0 & \cdot & \cdot & 0 & & & & \\ 0 & 1 & \cdot & \cdot & 0 & 0 & 1 & \cdot & \cdot & 0 & & & & \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & & & & \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & & & & \\ 0 & 0 & \cdot & \cdot & 1 & 0 & 0 & \cdot & \cdot & 1 & & & & \end{array}\right] \\ \underbrace{\qquad\qquad\qquad}_{\text{Identity matrix}} \quad \underbrace{\qquad\qquad\qquad}_{\text{Identity matrix}} \quad \underbrace{\qquad\qquad}_{\begin{array}{c}\text{Each row contains 2} \\ \text{unities and } M-1 \text{ zeros}\end{array}} \end{array} . \tag{10}$$

Matrix (10) shows that, out of the $5N+1$ scales to be determined, only $N+M+1$ can be independently specified. The independently specifiable scales correspond to those columns in (10) which, when deleted, leave a nonsingular matrix. It is also evident that a nonsingular matrix, and hence unique values for all scales, can always be produced by leaving either all the α's or all the β's (or a mixed set of N α's and β's) unspecified. This scheme, however, is of little value, since it is always desirable to preserve the freedom of specifying as many α's and β's as possible, so that optimal scales can be guaranteed at the outset. It is also imperative to be able to specify ϵ_0 independently, since this scale constitutes the only means by which the speed of computation can be directly controlled. Thus, the task at hand is to find in (10) a nonsingular $N \times N$ matrix, which contains the least number of α and β columns and which does not contain the ϵ_0 column.

The ϵ Matrix

The best one can do to establish optimal scaling is to find in (10) a nonsingular matrix which contains all the ϵ columns exclusive of ϵ_0. Since $M<N$, it is always necessary to augment the ϵ columns with at least one α or β column; hence, complete optimality can never be guaranteed. As will be shown below, the α or β augmenting columns can be determined with the aid of the "ϵ matrix"—the portion of matrix (10) to the right of column ϵ_0. As an example, (11) shows the ϵ matrix for the problem of Fig. 2.

$$\begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 5 \end{array} \\ \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ -1 & 1 & 0 \\ -1 & 1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \end{array}. \tag{11}$$

Any $M\times M$ nonsingular matrix constructed by deleting $N-M$ rows from the ϵ matrix will be called a "reduced ϵ matrix." If rows $i, j, \cdots$ are the rows deleted from the ϵ matrix to form the reduced matrix, then α_i or β_i, α_j or β_j, $\cdots$ are the columns to be attached to the ϵ columns to form a nonsingular matrix. Consequently, α_i or β_i, α_j or β_j, $\cdots$ are the scales which should be left unspecified, while the remaining α's and β's are the scales which can be independently prescribed. Since the α's and β's play identical roles with respect to the scaling process, it is immaterial whether the α_i or the β_i is left unspecified. For simplicity, therefore, it will be assumed that at the outset all the β scales are specified according to the criterion of (2).

$$\begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 5 \end{array} \\ \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \end{array}. \tag{12}$$

Matrix (12) represents a possible reduction of (11). In this example α_3 and α_4 are to be left unspecified. After specifying ϵ_0, α_1, α_2, α_5 and all the β's, (8) can be used to solve for ϵ_1, ϵ_2 and ϵ_5, and subsequently for α_3 and α_4. After determining ϵ_3 and ϵ_4 through (7), all the γ's and δ's can be found through (5) and (6) respectively.

The generalized outline for the above procedure is:

1) Using the topological constraints of types 1) and 3), eliminate from the equilibrium constraints all γ's and redundant ϵ's.
2) Form the ϵ matrix.
3) Find a reduced ϵ matrix.
4) Specify ϵ_0, all β's, and those α scales which are indicated by the rows of the reduced matrix. ϵ_0 is to be specified according to the desired computation speed, and the α's and β's according to the criteria of (2) and (3), respectively.
5) Using the specified quantities with the ϵ matrix and the topological constraints of type 3), evaluate all ϵ's and unspecified α's.
6) Using the topological constraints of types 1) and 2), evaluate all γ's and δ's.

Manipulations of the ϵ Matrix

Every row in the ϵ matrix contains at least two unities (positive or negative); the rest of the elements are zero. Since there is always an independent variable, there will be at least one row containing a single unity. These properties imply that if a nonsingular ϵ matrix exists at all, it can always be found as follows. Select a row with a single unity; then select N-1 rows successively, such that each additional row will contain a unity in exactly one column which is zero in all the previously selected rows. Thus, a reduced ϵ matrix can be found directly with no need for exhaustive search. It can also be seen that, once the reduced matrix is constructed, evaluating the ϵ's does not entail simultaneous solution, but can be done recursively by proceeding from one row to the next, in the order of their selection.

In most problems the choice of rows in the above reduction scheme is not unique, in which case more than one set of specifiable α's will be available. Correspondingly, there may be several sets of solutions for the α scales. In matrix (11), for example, the selected rows may be 1-2-5, 1-3-5, 1-4-5 (where row 1 is the starting row), 2-3-5, 2-4-5 (where row 2 is the starting row).

The facility in which the reduced ϵ matrix and a corresponding set of scales can be produced is quite advantageous, since no solution is guaranteed to be adequate even if it does satisfy the equilibrium and topological constraints. It may happen that one or more of the unspecified α's come out lower than the value given by (2), in which case overflow will occur before the computation terminates. Additional difficulty may be caused by the fact that the range of the scales is limited by the size of the registers, and that the difference $\alpha_i-\delta_i$ ($i=1, 2, \cdots, N$) has to exceed a certain bound. In practice, these restrictions, which may be called "boundary constraints," are considerably less severe than the constraints previously discussed, since they involve inequalities rather than equalities. If the boundary constraints are violated by the first reduction of the ϵ matrix, a second one has to be carried out, and the process repeated until these constraints are satisfied. If no reduction yields a satisfactory set of scales, the values specified for the specifiable α's have to be raised, and the entire process repeated. Since no simplified procedure has been found for these cases, the search for scales here has to be done exhaustively.

In the above discussion it was assumed that the ϵ matrix can always be reduced. This assumption is not

valid for the relatively rare problems in which the integrating packages can be divided into groups coupled only through dy inputs. When this is the case, it is necessary to substitute one or more of the ϵ columns with α columns before a reduced matrix can be formed. Clearly, not more than M columns need to be replaced under any conditions.

Automatic Scaling Routine

The procedures described in the previous sections can be programmed as a scaling routine to be executed by a digital computer. The initial data required by this routine are the topological interconnections, the desired computation speed, the integrand maxima and the constant multipliers for all the integrating packages. The output is a compatible set of $5N+1$ scales.

The specification of the optimal α scales requires the knowledge of the maxima of all the integrands. Quite often this information is available only after the problem is run on the DDA. This difficulty can be resolved by first guessing the maxima and letting the routine compute a set of scales based on these guesses. After the first problem run, an inspection of all the integrands can serve to improve the previous guesses and consequently to yield more satisfactory scales. After several cycles, the scales will achieve their optimal values, and the DDA its most accurate mode of operation for the given problem. This iterative exchange of information between the scaling routine and the DDA is especially convenient when the analyzer at hand operates in conjunction with a general-purpose computer. Usage of a general-purpose computer for both scaling and problem running is also possible; such an operation, however, is seldom advantageous, since general purpose programs for the solution of differential equations are generally slower and more difficult to compile than corresponding DDA programs.

Conclusion

At present, all scaling operations for DDA's are done manually, by trial-and-error methods. This severely limits the usefulness of large-capacity DDA's (containing 100 or more integrating packages) which are available today. The above discussion shows that a compatible and optimal set of DDA scales can be produced systematically. In many practical problems the systematic scaling is direct and does not require an exhaustive search. In more difficult problems, the searching process can be considerably facilitated by the usage of a general purpose digital computer.

Acknowledgment

The author would like to thank the Bendix Computer Division of the Bendix Aviation Corporation for making this project possible, and Prof. Harry D. Huskey of the University of California for his useful suggestions and continuous encouragement.

Russian Visit to U. S. Computers*

E. M. ZAITZEFF† and M. M. ASTRAHAN‡

Part I—Negotiations

M. M. ASTRAHAN

Summary—**In April and May, 1959 an exchange of visits by computer experts took place between the U.S. and the U.S.S.R. This article will describe the series of negotiations which led up to this exchange and will also describe the visit of the Russian delegation to America. The visit of the U.S. delegation to Russia will be reported separately in a joint article edited by Willis Ware that will appear in the March, 1960 issue of these TRANSACTIONS.**

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THE exchange had its beginning late in 1957 when a group of Russian scientists requested visas to attend the Eastern Joint Computer Conference in December of that year. The State Department asked the IRE to make arrangements for an exchange under the assumption that a return invitation would be forthcoming. A U. S. group was selected quickly and alerted to the possibility of leaving on short notice to visit Russia. However, there was not enough time left before

the conference for such arrangements, no invitation was received, and the whole idea was given up.

At a meeting in December, the National Joint Computer Committee reviewed the history of this proposed exchange. It was agreed that such an exchange would be desirable and that the NJCC was the proper agency to promote it. We voted to invite a Russian delegation to attend the 1958 Eastern Joint Computer Conference in Philadelphia in December and also to visit U. S. computing installations and factories. In return we would expect an invitation for a U. S. delegation to visit similar installations in the Soviet Union. As NJCC Chairman, I undertook the task of conducting the negotiations.

My first step was to contact the State Department. The person there most directly involved in the cultural exchange program is Miss Ellen Gavrisheff of the East-West Contacts staff. From Miss Gavrisheff I learned what every host of a Russian delegation should know. We would be responsible for making travel arrangements, securing a guide and interpreter, getting approval from the places to be visited and watching out for closed areas. All arrangements are on a reciprocity basis, and the itinerary for each delegation must be agreed upon before the start of the exchange.

With the help of a State Department listing of some of the places we might wish to see in Russia, the NJCC Executive Committee drafted a letter to the U.S.S.R. Academy of Sciences suggesting the exchange. This letter was sent in April, 1958, and a follow-up was sent several months later, but no reply was received. Meanwhile, John Carr III had succeeded in inviting four Russian scientists to attend the annual summer conference on digital computers at the University of Michigan, Ann Arbor. The Soviet group was in the U. S. from June 16–30, and lectured at the University of Michigan and visited several other universities and commercial installations. In August, 1958, John Carr, Alan Perlis, James Robertson, and Norman Scott visited a number of computing centers and laboratories in the Soviet Union where they lectured on U. S. computer developments. They discussed our exchange proposal with Academician Lebedev who is the senior computer man in the U.S.S.R. Academy of Sciences and director of the Institute for Precision Mechanics and Computing Techniques.

At John Carr's suggestion, I cabled my invitation directly to Academician Lebedev and followed it up with a registered letter. This occurred in October, 1958. Within a week I received an answering wire which was the start of what has turned out to be quite an extensive correspondence by wire and letter. The wire was from A. V. Topchiev, Vice-President of the U.S.S.R. Academy of Sciences. Not only was it in Russian, but also the Russian characters had been transliterated into English, complete with transmission errors; thus I had quite a problem getting this first wire translated. Fortunately, Miss Gavrisheff can translate mispronounced transliterated Russian by phone. I have since been studying Russian and have progressed to the point where, with the aid of a good dictionary, I was able to translate the last wire in the chain myself. This proves that delegation exchanges are educational.

The first wire asked for information about the Eastern Joint Computer Conference and suggested that the Russians would like to see the NORC, TRANSAC, and IBM 704 and 709 machines. Nothing was said about a return invitation. With the assistance of Harry Goode, who is now chairman of the NJCC, I began to line up places to show the Russian delegation. As time passed, we had to forget the EJCC in December and think only about visits to various places. Fourteen telegrams and four letters later, counting messages in each direction, we were ready to meet the Soviet delegation in New York. This includes only the overseas communications; the arrangements within this country consumed much more paper and telephone tolls. Much trouble was saved by asking one person at each place to be visited to handle the tour organization, and one in each city to handle hotel arrangements. I would suggest that anyone considering organizing such an exchange should take full advantage of the experience now available. I will be happy to pass on this experience in more detail to any such person.

The Bendix Systems Division made E. M. Zaitzeff available to act as guide and interpreter for the group. He was selected because of his excellent command of Russian and his familiarity with computers. We met in New York on April 18, the day the Russians were expected. However, they missed a connection in Amsterdam and all that we knew was that they did not get on the plane. We had no way of knowing if they were still coming or not. Sunday morning, April 19, we got word that they were on the plane that day and so Mr. Zaitzeff and I met them at the airport that night. We were accompanied by Professor and Mrs. L. Bers. Professor Bers, a mathematician from N.Y.U., was to be interpreter for our delegation to Russia.

Part II—The Visit

E. M. ZAITZEFF

ONLY seven of the eight expected delegates arrived in New York. The eighth, Vsevolod Sergeevich Burtsev, whom I had an opportunity to meet a year ago at the Summer Computer Conference at the University of Michigan, was not among those who arrived. The group included the following.

Sergeiy Alekseevich Lebedev, a member of the Academy of Sciences of U.S.S.R., and the Director of the Institute for Precise Mechanics and Computational Techniques. Academician Lebedev was involved in developing the MESM (small electronic computer) while in Kiev, and in developing and constructing the bigger Soviet computers BESM I (big electronic computer) and BESM II, which is to be put into production. He was the official head of the group.

Vitaliy Arsenievich Ditkin, the Assistant Director of the Academy's Computing Center in Moscow. Dr. Ditkin heads a Mathematical Tables and Nomograms Group involved in calculation of tables by special functions. Dr. Ditkin also serves as the editor of *Vycheslitelnaja Matematika* (*Computational Mathematics*). He is a mathematician by education and his interests are in operational calculations.

Yuriy Yakovlevich Bazilevskiy, an engineer and a member of the Committee of Radio Electronics. Mr. Bazilevskiy headed the design of STRELA I and III, and has supposedly worked on the development of a URAL computer. His interests seemed to be quite broad, ranging from the design of computers and synthesis of automata, to the production techniques used in building of computers.

Sergeiy Nikitovich Mergelyan, a member of the Academy of Sciences of Armenia and corresponding member of the Academy of Sciences of U.S.S.R. He is a mathematician by education and his interests lie in theory of functions, a subject about which he read lectures for two months in Italy at the University of Rome. At present, he is the Director of the Institute of Electronic Computers in Erevan, Armenia. Three new computers are being developed at his Institute: EREVAN, which is a tube machine, ARAGATZ, which is also a tube machine, and RAZDAN, which is going to be the first fully transistorized Russian machine.

Viktor Mikhailovich Glushkov, a corresponding member of the Ukrainian Academy of Science and a mathematician and physicist by education. His interests in mathematics were in group theory and other modern algebra subjects. He was also interested in machine learning and net synthesis. At present, Dr. Glushkov is the Director of the Kiev Computing Center and a professor on the faculty of Kiev University.

Victor Semenovich Petrov, Director of the Moscow Computer Factory. Most of the machines built there, according to Mr. Petrov, are the analog-type machines, but some digital machines are also being constructed. Very little information on his factory could be obtained from him.

Vladimir Stepanovich Polin, an engineer in the Institute directed by Lebedev. His education was in molecular physics, but his present interests are in machine translation. His job is to work on a special machine design to be used for translation only.

The group was taken to a New York hotel. There they discussed their flight, after which Academician Lebedev brought up the question of their itinerary. He said he was quite happy with the arrangements with the exception of one major point. He felt that a longer visit should be scheduled to the IBM factory. He stated that in his country changes of schedules such as this could be very easily and swiftly arranged. Dr. Astrahan stated that he would try his best to arrange an additional trip to IBM, probably at the end of the two weeks, in place of another scheduled visit.

Although the visitors must have been very tired, they then invited their hosts to a vodka and caviar party in one of their hotel rooms. After friendly conversation, a few arrangements were made for the last two days' stay of the group in New York, which would include dinner at Professor Bers' home, and also a Saturday trip through the stores on 5th Avenue conducted by Mrs. Bers. Then the group broke up and each retired to his room.

Monday morning was a dreary, rainy day, and since the Soviet group did not bring their overcoats with them, many complaints were heard about the people in Moscow who had been in the United States before and who had talked the present group out of bringing their overcoats.

The first stop after breakfast was to be the building on Park Avenue in which the Soviet representatives to the United Nations are located. After some formalities were completed, the group was taken to a branch of the First National City Bank to cash their drafts. To everyone's disappointment, it was found that these drafts could be cashed only in the main office located on Wall Street. Since the group was expected in Poughkeepsie by 1:30 P. M. that day, time was running out. We decided to check out of the hotel and pick up the cars which were rented for the trip to Poughkeepsie. Somehow in the confusion, the first cab took off without any English speaking individuals inside. Dr. Astrahan and I found ourselves with the rest of the group in the second cab. Thus, upon arrival at the Hertz office and after paying off the cabs, we found that Mr. Glushkov forgot his briefcase in the cab, not knowing that this was the final stop, and thinking that the cabs would be

used to take us all the way to Poughkeepsie. Everyone became even more concerned when we were told that it contained three bottles of vodka and about six pounds of black caviar. It was never found.

In two rented cars the group was taken to Wall Street. It was about 12:00 noon when the two cars left Wall Street and headed north to Poughkeepsie where we were due in an hour and a half. After being separated on the Taconic Parkway, we each thought the other was ahead and were almost arrested for speeding. We were reunited by a flat tire as the police closed in, and all was well!

IBM

At IBM, the group was met by D. F. Ammerman, Assistant General Manager; Louis Voerman, Manager of Manufacturing; Ralph L. Palmer, Manager of Product Development; Dr. Frederick P. Brooks, Advisory Engineer to the Product Development Laboratory; and Thomas B. Eschenbrenner, Administrative Assistant to the Director of Research, who came in from New York, and was responsible for the arranging of the group's stay at IBM. Also available to help in translation were Thomas B. Farrely, IBM Field Representative, and Wayne Kalenich, Research Librarian. Mr. Farrely studied Russian in school, and Mr. Kalenich, being Slav, had quite a good grasp of the language. After exchanging formalities in a conference room and introducing everyone, the group was taken on a tour of the main plant.

The first stop of the plant tour was at the 705 installation where a number of group pictures were taken. These photographs were later given to the visiting group. From the 705 installation, the tour went to the third floor of the main building where a magnetic core matrix assembly was demonstrated. Many questions were asked in relation to this technique. Another point that interested the visitors was the programmed printed card component assembly machine which was operating at the time. The main 704 and 705 computer assembly line was shown, including also a 7090. Then the working day at IBM was finished and all the employees on the line left. A short stop at the transistor manufacturing room concluded the tour, and the group returned to the conference where a few questions were asked by both sides. Questions on the reliability of IBM computers were asked most often. Next were questions about the tape unit, tape interchangeability, and way of writing information on tape to insure reliability.

After dinner, the group was taken by Dr. Astrahan to the private homes of some of his friends at IBM. Finishing the long day, the group went to their motel, which, by the way, they liked more than any of the hotels they stayed in later.

The next morning, Tuesday, April 21, the group was driven to the IBM Research Laboratories Building 701, where they were met by J. E. Fellows and escorted to the conference room. There, after greeting and orientation by Dr. L. P. Hunter and Dr. E. R. Piore and after exchange of formalities and presentation of the Russian books and papers which were brought by the group, the group was taken on a tour of the Magnetics Department Laboratories. The tour was conducted by E. W. Pugh. Questions on magnetic films and ways of depositing magnetic material onto films were asked. After the tour of the Magnetics Department and a coffee break in the cafeteria, the group was led to the Computing Center where a 704 installation was examined. An experimental learning program for playing checkers was demonstrated and Professor Ditkin played against the machine. After a number of moves, the machine conceded. J. L. Ravesloot conducted the tour through the Computing Center.

A short lecture on machine learning was given by Dr. B. Dunham in the auditorium and a number of questions concerning the subject were asked by V. M. Glushkov. After the lecture, the group was taken to the Semiconductor Research Laboratory where Gunther-Mohr described the work done at that laboratory.

After luncheon in the conference dining room, a question and answer period began. Most of the questions asked by the Russian delegation dealt with the reliability of the machines, the tape units and their construction and operation, the preventive maintenance used on computers during the construction phase and also after installation in the field, and the time it takes to assemble different types of machines. More questions were asked on the details of manufacturing as well as on the research conducted in the areas of new memories such as film, magnetic film, and cryogenics, the transistor research that is being done there including some of the data on the later types of alloy junction and drift and diffused base transistors. In return, the members of the visiting group answered questions of the IBM people which mostly dealt with the work being done in the U.S.S.R. in the fields of machine learning, translation, weather predicition as well as with the manufacturing of the machines. In machine learning, it was stated, very little work is being done with the exception of some industrial processing learning computers. As far as the translation of language is concerned, the special purpose machine is believed to be the solution as far as the Russian scientists are concerned. At present, they are doing work on theoretical research of the languages to be translated and, to some extent, they are forming specifications for the special purpose machine to be built when sufficient background work has been done. Some work in establishing a system for abbreviation to be used in the translation machine is being done. This would decrease the necessary size of the memory. Also, ideas about the organization of such a machine are checked and tested. In the field of weather prediction, the group stated that they have a special purpose machine called POGODA (which means "weather" in English). They use this machine for long-term prediction for a month and short-term prediction for 24 hours. The monthly prediction is regular; the 24-hour prediction is less regular, making on the average of two predictions a week. The data for prediction is taken from three layers and it takes about half an hour for the computer to run

through the program. To the questions on how many points the data is taken from, Academician Lebedev stated that he did not know.

An additional plant tour of the production facilities was scheduled for the last Friday as well as an afternoon question and answer period. The members of the group were quite pleased to hear that they would be allowed to return to IBM for another day and assured Dr. Astrahan that they would do everything in their power to arrange for the American delegation to visit Erevan, a city not on the original schedule. At about 4:30 P. M., the conference ended and the visiting group was taken to the LaGuardia Airport where they boarded a plane to Boston. Dr. Astrahan separated from the group at this point and went back to San Jose, Calif., where he is employed. I was left alone with the group to continue on the trip.

M.I.T.

At the Boston Airport, we were met by Dr. Frank Verzuh and Mrs. Verzuh of M.I.T., who helped in getting out the luggage, hiring the cabs, and supervising the loading of the cabs which was one of the more difficult parts of the job for me. The group was taken to the Sheraton-Plaza Hotel and checked into their respective rooms.

Early the next morning, the group left in two cabs for the M.I.T. campus. The weather was chilly and coats certainly would have been desirable. Professor Philip M. Morse, Director of the M.I.T. Computational Center, started the day with a short presentation of the work done at M.I.T. in the Compton Laboratories. Some questions by the visiting group about the structure of the organization at M.I.T. Compton Laboratories were asked and a detailed block diagram was drawn for them on the board. Prof. Morse and Dr. Verzuh, who is Assistant Director of the Computation Center, Prof. Dean N. Arden, Prof. John McCarthy, and Dr. Fernando J. Corbato were present during the morning discussion. After the exchange of some of the printed material brought by the Russians and some of the paper distributed to the Russians by Dr. Verzuh, the group was taken to the IBM 704 installation where a number of effective programs were demonstrated. M. Loren Bullock of the IBM Corporation conducted the tour through the installation.

Lunch was served at the Faculty Club, where the group was joined by Prof. Dudley A. Buck and Douglas T. Ross. Also joining the group were Benjamin M. Gurley and Irving L. Levow from the Lincoln Laboratories staff. When the visiting group found out that Prof. Norbert Wiener was in the building, they asked if it would be possible to see him. Especially interested in seeing him was Mr. Mergelyan who had met Prof. Wiener previously in India during one of the Conferences attended by both. Prof. Buck volunteered to locate Prof. Wiener. Mr. Mergelyan's English which is quite good allowed the two to converse about their present work without the need of the interpreter but the conversation was so enthusiastic that when the lunch was over, Mr. Mergelyan's plate had not been touched. This was one of the few lunches when I managed to finish my meal. I usually had to time-share eating with being an information flow channel.

After lunch, Prof. Buck took the group to his Cryogenics Laboratory where an explanation of the work done there was given. Unfortunately, the containers for the liquid helium used for cooling the cryogenic materials were being refilled and no actual demonstration could be given. Nevertheless, a very detailed and comprehensive explanation of the work was presented. The Russian group was quite interested in the way the helium is saved in operation in the laboratory and were surprised to learn that this is not being done. Since helium is quite cheap in the United States, there is no necessity for saving it at the present time. On the other hand, in Russia helium is not found in natural state and thus it is imperative that it be circulated without a large loss of the gas during the experiments.

From the Cryogenics Laboratory, the group was taken by Douglas T. Ross to the Servomechanisms Laboratory where they were shown a computer-controlled milling machine and the work done by it. Some papers describing the work of the milling machine were passed out to the visitors.

The next stop on the tour was the TX-0 computer installation on which a simple pattern recognition program was demonstrated. The program is a learning type program which, during the course of experimenting, is supposed to improve its ability to decide between an x and a 0 drawn on a cathode-ray tube face with a light pencil. The results of the experimenting by the visiting group was satisfactory until the sizes of x's and 0's decreased to the point where the machine seemed to guess randomly as to what figure was drawn. After close examination of the TX-0, the group went to the conference room where the TX-2 computer was described to the visitors. Unfortunately, they could not see the actual computer but were shown some of the photographs and given the basic facts about it by the people from Lincoln Laboratories staff. The air-conditioning system of the Compton Laboratories was closely examined by the group; special interest was shown in it by Mr. Petrov and Mr. Bazilevskiy who seemed to be interested in a variety of topics. Most of the questions asked that day were of the type asked at IBM with some additional subjects touched. For instance, many questions were asked about the structure of the organization at the Compton Laboratories, the procedure that is taken in solution of the problems, how they are prepared and how they are solved, and how one obtains time on the machine. Also, some questions were asked on the translation activities at M.I.T. and on the pattern recognition work done there.

After dinner at a nearby restaurant, the group was invited to the home of Dr. Frank Verzuh. Only Lebedev, Petrov, Bazilevskiy, and I went to the Verzuhs' where we spent a very congenial evening. An interesting statement made by Mr. Petrov during the evening was quite memorable. He said that he felt, after spending three

days in the United States, that Americans were probably the people whose interests were closest to the Russian people and he felt that they could talk about more things of common interest than with any other nationality he had met in his previous travels; he added that before coming to the United States, they were warned that Americans would be suspicious of the visitors and probably quite uncooperative. This, he felt, was not true at all. In general, from the comments of the group made later, it was felt that the day at M.I.T. was very productive and enjoyable.

Harvard

The next day the group was taken to Harvard, where they were met by Prof. Howard Aiken, Dr. Anthony Oettinger, and other members of the Computation Laboratory. The group was taken to the conference room where a discussion ensued. Most of the discussion involved the structure of the Harvard Computation Laboratory. Later the group was taken upstairs where MARK I, MARK IV, and UNIVAC computers were shown. More discussions were held in individual offices. The visit concluded about 1:30 P. M. and the delegation was taken back to the hotel.

Philadelphia

That evening, the group was at the Boston Airport ready to fly to Philadelphia on Northeast Airlines. As the plane was being boarded, Dr. Lebedev and Mr. Polin were admitted to the aircraft but Mr. Petrov was stopped; the official at the gate stated that his reservation was not confirmed. I checked with the official and found that only two out of eight passengers scheduled to fly on that flight had their reservations reconfirmed. The plane was completely sold out and there was a long line of additional people waiting hopefully for a cancellation. Since I reconfirmed reservations for the whole group the previous day, it seemed very unreasonable that only two people would have their reservations. The suspicion was, of course, that the girl who was taking the confirmations gave up on the Russian names after two of them were read off and did not bother checking the other six. After a short discussion with officials at the airport, some finagling was done by the airline and everyone was allowed to get on board.

At the Philadelphia Airport, the group was met by Dr. Morris Rubinoff of Philco Corporation and the Moore School of Electrical Engineering of the University of Pennsylvania. Dr. Rubinoff was to be the host for the stay in Philadelphia.

AT 8:30 the next morning Dr. Rubinoff and Henry Sparks from the University of Pennsylvania came to pick up the group and take them to the campus of the University. The group was led to the conference room and greeted by representatives of the University of Pennsylvania, Burroughs, RCA, Leeds and Northrup, Philco, and Auerbach Electronics. The Russian group had stated their desire to see TRANSAC during their visit to the United States but the facilities of Philco where TRANSAC is being built are restricted because of government work. Therefore, the next best thing was done. This was a formal presentation on TRANSAC with colored slides, given by Dr. Rubinoff in the conference room of the Moore School. This presentation took most of the morning. After lunch, the conference continued with a description of RCA's 501 given by one of the representatives of that company and many questions were answered by the representatives of the other companies. Printed material about the S-2000 was given to the visitors.

The last part of the afternoon was used for American members to ask questions of the Russian group. In answer to the questions, the following facts were brought to light. The problem with skew in Russian tape units is quite acute. The tapes used range from $6\frac{1}{2}$ mm wide to 125 mm wide. Most common is the 35-mm tape which uses ten channels. The tapes range up to 1 km long but many of them are shorter than that. The average speed of the tape is between 2 and 4 meters per second. Most of the Russian machines are binary machines that do not have alphanumeric inputs. The reason, they state, is that all their machines are used for scientific problem solutions and very little data processing is done. Drums are used quite extensively and the majority of them are horizontal type with 4 bits per millimeter packing density. They also stated that the prices of their equipment are much lower than our prices. Comparing the drums for instance, they felt that a drum four times as large as the one described to them would cost half the price of the American drum; thus a factor of 8 is involved. This, they believe, is because no research time is charged to the drum purchaser. The printers they described are operated up to 20 lines per second which is equivalent to 1200 lines per minute. These printers have a tolerance of 0.2 to 0.3 millimeters of up and down motion in lining up a line.

Other computers they touched upon were the VOLGA, which is a general purpose computer and not yet completed; POGODA, which is the weather prediction computer (special purpose); CRYSTAL, which is a special purpose machine for investigation of crystal structures; GRANIT, which is a special purpose machine for statistical investigations; the EREVAN, which is a tube machine and not yet completed; ARAGATZ, also a tube machine named for a mountain in Armenia (this machine also is not completed); and RAZDAN, a transistorized machine being developed which is named for a river in Armenia. The last three computers are being designed with printed card circuitry and micro components; the construction is patterned after the type of IBM units where memory, arithmetic unit, and other large size units are separate from the main installation and can be interchanged between installations. The M-series machines, M2 and M3, were also mentioned. No detailed information about any of these machines was given. In reply to a question about industrial processing control by computers, three types of systems were superficially described: a computer controlling the temperature and

power of the melting of metals, a chemical process computer, and a computer installed on a train which considered the weight of the particular train, the profile of the terrain, and the time table it had to meet in computing the most efficient speeds at different points of the track. Some questions on the reliability of computers were raised and the delegation asked if there were any figures on the difference of good time on computers, depending on whether preventive maintenance was done or not. Figures were given on the UNIVAC at the University of Pennsylvania, where it was stated that 95 per cent good time was obtained with maintenance and only 88–91 per cent good time was obtained without maintenance.

In Philadelphia, before boarding the train for Washington, the group was taken for a few minutes to Independence Hall, where a very cooperative guard played a record of the Liberty Bell's history and showed the room where the Constitution was signed. After this they were taken for a drive through the city with explanations of the buildings and statues on the way to the railway station.

Washington

With the exception of a Saturday evening cocktail party and dinner given by the members of different organizations that the group was scheduled to visit the following week, the next two days in Washington were free for the group for sightseeing and shopping. The group's sightseeing during the weekend involved a 10-mile tour on foot of the downtown area on Saturday after a stop at the Soviet Embassy, and general sightseeing on Sunday, when some of the group were accompanied by Dr. and Mrs. John W. Carr, III.

NBS

Monday morning, April 27, the group was accompanied to the National Bureau of Standards by Capt. William Patterson of the U. S. Army, who is temporarily attached to the State Department and who was assigned to assist me during the stay in Washington. They were met by Dr. S. N. Alexander and taken to the conference room of the Division of Applied Mathematics, where Deputy Director Robert D. Huntoon gave a speech of welcome. The first part of the morning program was directed by Miss Ida Rhodes, who speaks Russian and who is connected with the Applied Mathematics Division where she is working on a machine translation of Russian into English. Most of the discussion dealt with the organization of the Division of Applied Mathematics of the National Bureau of Standards and the types of problems that are being solved or worked on in that division. Questions on different approaches to solutions of problems, as well as on the size of the problems tackled, were raised.

The second part of the morning was spent in the Data Processing Division of the National Bureau of Standards with Dr. Alexander, the head of the division. Two programs were demonstrated on SEAC, one in data retrieval which is to be used in finding chemical formulas to help in patent search, and the other, a program of character recognition which was demonstrated using Russian letters. After a close examination of SEAC, an air traffic control system that is being developed at NBS was also demonstrated.

Bureau of Census

For lunch, the group went to the Bureau of Census where a large UNIVAC installation was later shown, a model of FOSDIC explained, and samples of census cards passed out to the visitors. Many questions on the operation of FOSDIC were answered. From the Bureau of Census, the group was taken to the home of Mr. McPherson where a number of bottles of the Russians' vodka and cans of caviar were served. From there, the group was taken to the park for a picnic which unfortunately had to be held inside since it was raining. Later in the evening, the group was asked by Jacob Rabinow to visit the Rabinow Engineering Company. Mr. Glushkov and Mr. Polin, Harry Goode, Sam Alexander and I went to Rabinow Engineering. Since Rabinow speaks excellent Russian, no translation was necessary and a lively conversation lasted until midnight between Mr. Rabinow and the visitors.

NORC

On Tuesday, April 28, the group was scheduled to go to Dahlgren, Va. where they were met by Capt. Utgoff of the United States Navy who spoke to them in Russian. Reporters from two local newspapers were allowed to take some photographs which were later distributed to the visitors; after this a tour of the computational facilities of the Proving Grounds was made. The group was divided into two subgroups, one with me and the other with Capt. Patterson. The NORC installation was shown to the visitors and a number of experimental programs were run. A close inspection of a CHARACTRON was allowed. Samples of CHARACTRON prints were shown and were passed out to some of the visitors. Besides the actual NORC installation, the testing equipment for the packages and memory tubes were demonstrated. Also inspected were the generating facilities and cooling facilities for the installation. The repair shop and the preparation-of-data room using IBM equipment with card-to-tape converters was shown. The final stop before lunch was the Proving Grounds where the Automatic Data Translator which is being developed was seen.

Lunch was served at the home of Capt. Utgoff. After this, the group returned to the conference room where a question and answer period was held. Most of the questions and answers were of the same type as asked before at previous stops.

FAA

Wednesday morning, April 29, the group was taken to the Federal Aviation Agency where Commander LaLiberte, with Mr. Gruell, Mr. Fields, and Mr. Amberg, greeted the visitors. A formal presentation by Commander LaLiberte, with the help of Mr. Gruell and

Mr. Fields, was given on the Federal Aviation Agency's air traffic control program. The presentation included graphs and slides, and a set of booklets and reports on the program were distributed to the visitors. An additional discussion by Saul Amberg on the computer that is to be used in the program followed. A short question and answer period was held during which the Russians stated that, unfortunately, they were not too familiar with traffic control and that no program of that type, so far as they knew, exists in their country.

Patent Department

From the FAA, the group walked to the Bureau of Patents where they were greeted by Robert Watson, Commissioner of Patents, and D. V. Andrews, Director of Research and Development. After lunch in the building of the Bureau of Patents, the group went on a tour, conducted by the Commissioner, of the Patent Library and then was led to the conference room where Mr. Andrews gave a formal presentation of the work in computational technology being conducted at the Bureau of Patents. Three approaches to the work were described. They included the punched card approach, the ILAS and RAMAC. After the description and a question and answer period, the RAMAC installation was shown, with the experimental program demonstrated. There were offers to show other methods but they were of no interest to the visitors.

Thursday, April 30, was scheduled to be a free day during which the group was to spend their time shopping in Washington, D. C. Capt. Patterson and I were asked to be of assistance in their shopping tour. Most of the items bought consisted of clothing for their wives and children, a few items for their families, and very little for themselves. Most of the members of the group bought foldable raincoats. That evening the group left by train for New York.

IBM Again

The next morning, May 1, Academician Lebedev, Mr. Bazilevskiy, and Mr. Petrov were taken to the IBM installation in Poughkeepsie while Prof. Ditkin and Mr. Mergelyan were invited to give lectures at the New York University; Mr. Polin and Mr. Glushkov remained in New York City to straighten out details of their return trip to Russia. The group was met at IBM by William Mair, General Manager and Vice President of the Company, along with other personnel who were active in the previous visit of the Russian group to IBM. After a short discussion, the group was taken on a tour through the plant where they were shown the pressing of the magnetic cores, the mixing of core powders, the firing ovens for the cores, and the automatic testing equipment for testing of the core parameters. They were given temperatures and other parameters of interest. Then the group was led to the magnetic head assembly section where they were shown the complete process, starting from the individually stamped plates to the final assembly and polishing process. They were also conducted through the magnetic tape drive mechanisms assembly line and their testing setup. The group was given a demonstration of how magnetic memory matrices are checked by special equipment to determine whether the cores are all in proper position. Continuity checking of packages was shown and individual package testing by hand methods on tube packages was demonstrated. The automatic programmed printed card assembly machine was shown again, but it was out of operation at the time; each visitor received printed material on its description. Also received as souvenirs were small stamped plates from which the magnetic read and write heads are assembled, the paper forms on which the description of each individual core matrix memory is recorded and the paper forms on which the history of tube packages are recorded. Since the group was much smaller this time, much better understanding of the operation of IBM facilities was possible, more questions could be asked and answered more thoroughly, and a more detailed observation of the process could be made. The lunch was served at the IBM Homestead after which Mr. Mair took the group out to the golf course behind the Homestead and showed them the elements of the game. Each of the visitors had a chance to use a 9 iron and putter later on the green. To the great delight of everyone present, they were quite good, considering that none of them had ever held a golf club before.

After lunch, the group returned to the main plant where the painting process used in painting the cabinets for IBM equipment was shown from the beginning stage, when paint is mixed, to the final stage when it is dried. A short discussion in the conference room followed, after which the group started back toward New York. On the way out of town, they were asked to stop at the IBM Country Club which was thoroughly examined, inside and out. All of the members of the party on the visit to IBM for the second time were quite impressed with their hospitality and the amount of information received there. In the words of one of the members of the group, they had a chance to see the whole factory from top to bottom.

That evening the group went to see Cinerama. Their comments on the comparison of Cinerama and the Russian equivalent were that the colors of American movies were very good, possibly better than theirs, and that the solution of the line problem where the three projected images meet each other has probably been solved better here than in U.S.S.R. Nevertheless, they felt that the direction was inferior to the direction of the Cinerama films made in Russia.

Saturday was spent in sightseeing and shopping in New York. Saturday evening the group was invited to a dinner party at Professor Bers' home. Sunday was spent sightseeing in New York. Professor Bers took the group to the International Airport where they boarded the plane for Amsterdam and Moscow.

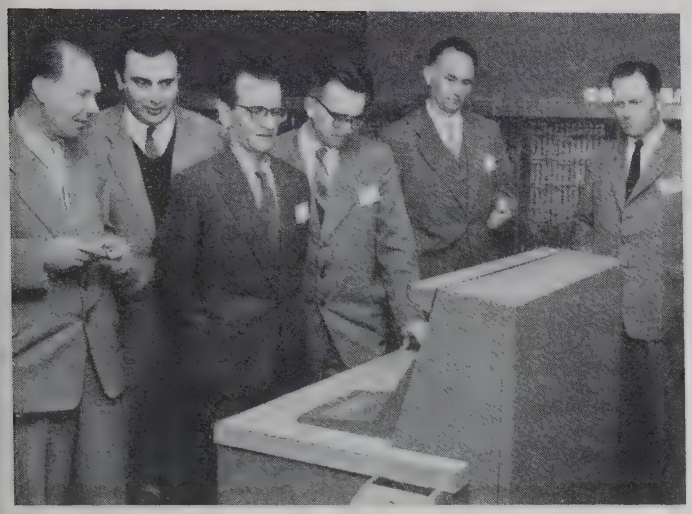


Fig. 1—At the 705 Console in Poughkeepsie. Left to right: Polin, Mergelyan, Lebedev, Glushkov, Bazilevskiy, Petrov.

Fig. 2—At the country club in Poughkeepsie. Right to left: Lebedev, an IBM host, Petrov, Zaitzeff, Bazilevskiy.

General Comments

In general, the group was quite cooperative and friendly with the interpreter. Most of them made comments about the friendliness of the American people with whom they had contact, and also stated that they did not expect so friendly a reception as they received. They were impressed with the area north of New York City, and stated that they never expected to find such beautiful nature so close to a city of the size of New York. They continually asked the number of the population in each city they visited and seemed to be unhappy when the answer was not known by the interpreter. They were surprised by the building activity in New York City and by the new skyscrapers that are going up. They had been told that skyscrapers are very inefficient, money is lost by building them, and thus that no skyscrapers were being built in America. Slowly, but finally, they were quite impressed by the cars, if not by the number, then by the construction and design of the vehicles. Prices of the cars were asked constantly and were not readily believed when the conversation involved used car lots. It seems that it would be advisable to take some other group that is coming here to a used car lot and actually show them the cars at close range with their prices.

Most of the members of the delegation, especially Professor Ditkin and Academician Lebedev, repeatedly stated that this type of exchange is very good and even if the political leaders of the countries might have some differences, he felt that the scientists should keep in contact with each other.

Washington impressed the group most of all as the cleanest and most beautiful city they had seen. The weather was also nice there, and not having coats, they appreciated this.

A few questions were asked about the salaries of engineers, programmers, operators of machines, and taxi drivers. The question concerning the taxi drivers came up in Boston where the answer they received from one was that he was making more than an average taxi driver since he owned his own cab! The Russians stated that this could not be true since he had a radio receiver in his cab; the taxi driver explained that five or six got together and organized their own small cab company with each owning his own automobile. This impressed the group.

I can give some advice to the organizers of future exchanges. Probably the most important point is the need for sufficient interpreters for tours of factories and computer installations. One interpreter for four or five people is about the minimum that can be advised. Also, when it comes to nontechnical activities such as checking into hotels, checking out of hotels, buying tickets at railroad stations, getting groups into cabs and walking around stores, no more than four people should be with each interpreter. Realizing that this problem is not very easily solved, a compromise suggestion could be offered where, at least, an American with no knowledge of Russian could be assigned to the group besides an interpreter if the group consists of more than four or five people. Since almost all Russians who come for a visit in the United States have some knowledge of English, an additional individual who does not speak Russian could be of great help in driving automobiles, checking into and out of hotels, taking care of bell hops and restaurant checks, and in being able to take the group on tours of the city. In places where such help was available for the above described tour, the tour went much more smoothly than when only one individual acquainted with American customs and procedures was present.

Disregarding small troubles and problems that were all fairly satisfactorily resolved during the trip, the trip went quite smoothly mainly because of very good detailed organization of the program before the arrival of the visitors. When the program was well worked out by the individuals responsible for the group at each stop, things were enjoyable for all parties.

Correspondence

An Accurate Bidirectional Transmission Gate Using Semiconductor Diodes*

The dc level of the B′ Integrator used in controlling the frequency of the accelerating voltage at the Princeton-Penn Proton Synchrotron must be maintained stable to within ± 0.01 per cent each cycle. This is accomplished by sampling the output of the integrator for 2 μsec, comparing this with a reference voltage, and then injecting into the integrator capacitor the amount of charge necessary to correct the error. An electronic transmission gate passes this charge and must have the following properties.

1) Rise and fall times of less than a few hundred millimicroseconds for a total ON time of 2 μsec. This is imposed by the synchrotron's magnetic field which is built up from 260 gauss to 15,000 gauss in 25 μsec.

2) When the gate is OFF its leakage current must be less than several millimicroamperes. This period is nearly 50 msec, and any leakage current will contribute to excessive drift of the dc amplifier which is to be stabilized.

3) The input to the gate will be no greater than ± 3 volts. A gate gain of unity is desired. Any output pedestal must be constrained to less than a millivolt.

These requirements were satisfied by an adaptation of the six-diode gate[1] shown in Fig. 1. Vacuum tubes were precluded from use in this application because of shunt capacitance, cathode-to-heater leakage, and large forward resistance (compared with semiconductor diodes). Recently, silicon junction diodes have been available with back resistances of several hundred megohms and extremely low forward resistance. The difficulty that arises in trying to use them for this application is due to the minority carrier storage resulting in comparatively long recovery time.

A satisfactory solution is shown in Fig. 2. Here diodes D_1, D_2, D_5, and D_6 are series combinations of the high-back resistance silicon junction type 1N459 and the fast germanium point-contact type 1N100. Diodes D_3 and D_4 are 1N100's alone since they need not have high back resistance. In this scheme the 1N100 presents a fair amount of back resistance to reduce leakage, while the 1N459 is recovering to its full back resistance.

This approach was first investigated by measuring the recovery charge in a 1N459 diode and in a 1N459-1N100 series combination. In the experimental arrangement of Fig. 3, a forward current of 10 milliamperes was used before switching the diode to the reverse polarity. The 1N459 alone recovered to 3 megohms in 12 μsec and transferred a charge of about 24×10^{-10} coulombs. The series combination of 1N100 and 1N459 transferred only 0.9×10^{-10} coulombs.

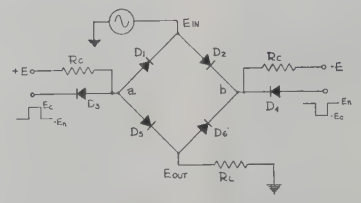


Fig. 1—Basic six-diode bridge gate from Millman and Taub.[1]

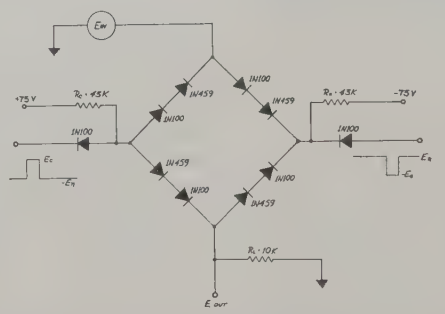


Fig. 2—Gate designed for the Princeton-Penn Proton Synchrotron.

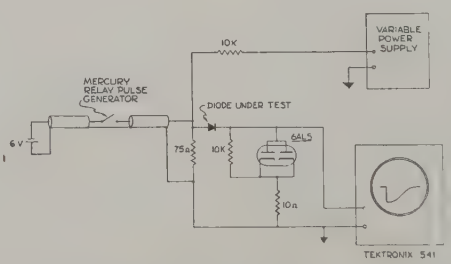
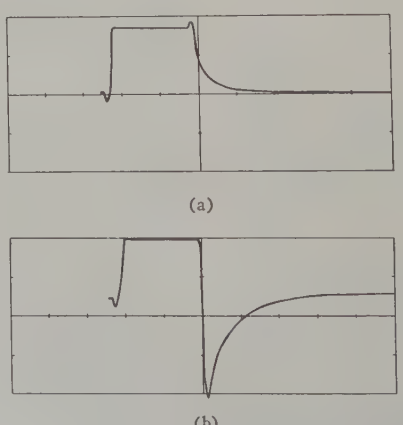


Fig. 3—Test arrangement for studying the switching behavior of a diode. The 6AL5 merely limits the voltage across the 10 K load resistor so that the entire waveform may be observed.



(a) (b)

Fig. 4—A +3 volt dc input gated for 2 μsec by (a) the gate of Fig. 2, and (b) a gate using 1N459's alone.

Comparisons were then made of the six-diode gate, using all 1N459's, vs the gate of Fig. 2. The results of a test in which 3 volts dc was gated for 2 μsec are shown in Fig. 4. Consistent with the aforementioned observations of leakage transferred by the individual units, the bridge with 1N459's alone transferred an excess of 5×10^{-10} coulombs while the circuit of Fig. 2 allowed 0.7×10^{-10} coulombs to pass after being turned off. The latter figure could probably be reduced further by speeding the switching time.

This gate, composed of high back resistance diodes in series with fast diodes, is suitable for passing small signals for short periods of time. The use of semiconductors, beside their desirable electrical properties, permits simple, compact packaging. It is realized that this approach is an interim measure awaiting the availability of the fast high back resistance diode.[2]

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* Received by the PGEC, April 16, 1959; revised manuscript received, September 10, 1959.

[1] J. Millman and H. Taub, "Pulse and Digital Circuits," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 445–447; 1956.

[2] E. G. Rupprecht, H. J. Patterson, and P. Miller, "Hyperfast Diffused-Silicon Diode and Transistor for Logic Circuits," presented at Solid-State Circuits Conference, University of Pennsylvania, Philadelphia, Pa., February 12–13, 1959.

Self-Dual Symmetric Switching Functions with a Certain a-Number Constraint*

This note is concerned with three significantly useful invariance properties of two-valued Boolean functions. It is shown that the class of two-valued Boolean functions satisfying the conjunction of these three properties is empty. For brevity we will hereafter refer to "two-valued Boolean function" simply as "Boolean function."

Definition 1: Let n be some positive integer. A Boolean function T of n variables is said to be *self-dual* if and only if

$$T(x_n, \cdots, x_1) \equiv T'(x_n', \cdots, x_1'),$$

where a prime denotes the complement of the Boolean function or variable concerned.

The motivation for the word "self-dual" in definition 1 comes from the topological significance of a switching circuit realization of T considered as a switching function.

* Received by the PGEC, July 6, 1959.

Definition 2: Let n be some positive integer. The complement of the *symmetric*[1] Boolean function $S_{\{a_j\}}$ of n variables is denoted by $S'_{\{a_j\}}$ and is defined by the identity

$$S'_{\{a_j\}}(x_n, \cdots, x_1) \equiv S_{\{\hat{a}_j\}}(x_n, \cdots, x_1),$$

where $\{a_j\}$ denotes some sequence of the so-called a-numbers[1] of the symmetric function and $\{\hat{a}_j\}$ denotes those members of the complete set of a-numbers $(a_0, a_1, \cdots, a_n)$ not present in $\{a_j\}$ where $\{a_0, a_1, \cdots, a_n\}$ is some permutation of $\{0, 1, \cdots, n\}$ and j is an integer satisfying the condition $0 \leq j \leq n$.

Lemma:[2] Let n be some positive integer. A symmetric Boolean function $S_{\{a_j\}}$ of n variables satisfies the condition

$$S_{\{a_j\}}(x_n, \cdots, x_1) \equiv S_{\{a_j\}}(x_n', \cdots, x_1'),$$

if the a-numbers satisfy the condition

$$\{a_j\} = \{n - a_j\},$$

where $\{n-a_j\}$ is the set of a-numbers found by replacing each a_j in $\{a_j\}$ by $n-a_j$.

Theorem: The class of self-dual symmetric Boolean functions of n variables with a-numbers satisfying the condition $\{a_j\} = \{n-a_j\}$ is empty, for every positive integer n.

Proof: Each of the three invariance properties is satisfied nonvacuously. In fact, with almost no ingenuity one can actually display specific examples of representatives from each of these classes of functions.

Assume the hypothesis and the negative of the conclusion of the theorem and arrive at a contradiction.

If such a $S_{\{a_j\}}$ existed for some positive integer n it would necessarily satisfy the following conditions:

1) By definitions 1 and 2,

$$S_{\{a_j\}}(x_n', \cdots, x_1') \equiv S_{\{a_j\}}(x_n, \cdots, x_1).$$

2) By the lemma,

$$S_{\{a_j\}}(x_n, \cdots, x_1) \equiv S_{\{a_j\}}(x_n', \cdots, x_1').$$

From 1) and 2) we arrive at the proposition that $S_{\{a_j\}}(x_n, \cdots, x_1)$ and $S_{\{\hat{a}_j\}}(x_n, \cdots, x_1)$ should be identical. But this is absurd, since by definition 2, they are precisely complementary.

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[1] C. E. Shannon, "A symbolic analysis of relay and switching circuits," *Trans. AIEE*, vol. 57, pp. 713–722; December, 1938.
[2] S. H. Caldwell, "Switching Circuits and Logical Design," John Wiley and Sons, Inc., New York, N. Y., p. 259; 1958.

Combinational Relay Switching Fields*

Introduction

This note concerns itself with one aspect of the author's researches on the physico-mathematical theory of biological computers.[1,2] The aspect to be treated here deals with some switching properties associated with brain functioning and establishes a context in which one may speak of a combinational relay switching field, which is to be interpreted as a *generalization* of a combinational switching circuit.

Theory

The discipline of stochastic switching circuits[3,4] is to be the point of departure for the development of the theory.

It has been shown[5] that the series-parallel and bridge network of identical stochastically specified relay contacts each constitute an error-reducing redundancy of components, when compared to a single relay contact. Consider an isovolumetric topological iteration process.[4] By this is meant the following: 1) an iteration of network topology using some element of the (nonvacuous) class of basic error-reducing network configurations, and 2) that each network component has a reliability function defined on some nonvacuous index set of real-valued parameters such that the product of the total number of components by each of these parameters is a constant.

By considering the circuit-reliability function,[4] which is a real-valued function of network topology and component reliability, in the limit (if the limit exists) as each parameter of the domain of the circuit-reliability function approaches zero, one is led to an entity that may be called a homogeneous isotropic combinational switching field. If one of the parameters under consideration is the volume occupied by a component, then we have produced an analogy similar to that of the transition from an electric circuit to an electric field. More important, we are now in a better position to bring mathematical analysis (real variables) to bear on some switching problems. As the probability of error for the defining channel[4] for the contacts approaches zero, the conventional switching properties come into evidence. With the idea put forth in this paper, the switching properties have been distributed according to some set of parameters, say component volume.

Generalization of this model to what may be called the inhomogeneous case consists of letting the probabilities of the defining channel for the relay contacts differ from one contact to another instead of being identical for all contacts. Generalization to the anisotropic case consists of using an iteration process that alternates among different elements from the class of error-reducing network configurations. In the latter case it has been shown by the author[2] that the circuit-reliability function is not improved, almost everywhere (in the mathematical sense), in contrast to the case of iteration with only one element of the class of error-reducing configurations; actually it is improved except for certain line segments of component reliability. However, even under these circumstances it is not too difficult to establish bounds on the circuit reliability corresponding to these bizarre line-segments of component reliability.

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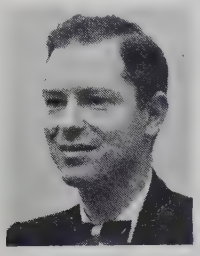
* Received by the PGEC, August 17, 1959.
[1] H. M. Von Foerster, *et al.*, "The Realization of Biological Computers," Elec. Engrg. Dept., University of Illinois, Urbana, Yearly Rept. for U. S. Office of Nav. Res.; January, 1959.
[2] H. M. Von Foerster, *et al.*, "Quarterly Progress Report Number 6 on the Realization of Biological Computers," Elec. Engrg. Dept., University of Illinois, Urbana; July, 1959.
[3] A. A. Mullin, "Reliable stochastic sequential switching circuits," *Trans. AIEE*, pt. I, vol. 77, pp. 606–611; November, 1958.
[4] A. A. Mullin, "Stochastic combinational relay switching circuits and reliability," IRE Trans. on Circuit Theory, vol. CT-6, pp. 131–133; March, 1959.
[5] E. F. Moore and C. E. Shannon, "Reliable circuits using less reliable relays," *J. Franklin Inst.*, vol. 262, pp. 191–208, 281–297; September-October, 1956.

Contributors



M. M. Astrahan

Morton M. Astrahan (S'45–A'50–SM'57), was born on December 5, 1924, in Illinois. He received the B.S.E.E. degree from Northwestern University, Evanston, Ill., in 1945; the M.S.E.E. degree from California Institute of Technology, Pasadena, in 1946; and the Ph.D. degree from Northwestern University in 1949.

He joined IBM Corporation in 1949. He participated in planning and logical design on the 701 computer in 1951–1952, was in charge of systems planning for IBM on the AN/FSQ-7 computer for the SAGE air defense system in 1953–1955, and directed input-output development and prototype testing for the AN/FSQ-7 in 1956. From 1956 to 1958, he was manager of San Jose Systems Research, where he was responsible for applications and specifications of experimental research devices for future data processing systems. Since 1959, he has been manager of systems development, San Jose Laboratory of IBM Advanced Systems Development Division, San Jose, Calif.

Dr. Astrahan was first chairman of the IRE Professional Group on Electronic Computers, 1952–1953; chairman of the National Joint Computer Committee, 1956–1958; and chairman of the NJCC Delegation visiting computers in the USSR in 1959.

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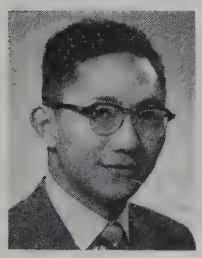


H. Chang

Hsu Chang was born in Yangchow, Kiangsu, China, on February 3, 1932. He received the B.S.E.E. in 1953, from National Taiwan University in Formosa, the M.S. degree in 1957, and the Ph.D. degree in 1959, from the Electrical Engineering Department at Carnegie Institute of Technology, Pittsburgh, Pa.

He joined IBM Research in Poughkeepsie, N. Y. in March, 1959. His current interests are magnetoresistive devices and investigation of garnet materials.

His past experiences include teaching at National Taiwan University, 1954–1955, and summer employments at Bell Telephone Laboratory, Murray Hill, N. J., and IBM Research Laboratory where he worked in the field of magnetic memory devices.

Dr. Chang is a member of Phi Kappa Phi and Sigma Xi.

❖

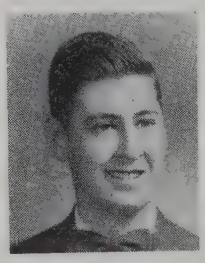
Winfield J. Giguere (M'57) was born in Claremont, N. H., on June 20, 1930. He received the B.S.E.E. degree from the University of New Hampshire, Durham, in 1954.

He joined the technical staff of Bell Telephone Laboratories, Inc., Murray Hill, N. J., in 1954. His first work was in engineering and development of carrier systems, microwave networks, and methods for diode measurement. More recently, he has been concerned with transistorized radio equipment and radio transmission. He is now engaged in exploratory development of circuits for a high-speed pulse-code-modulation system. Mr. Giguere was a winner of a Westinghouse Achievement Scholarship, was a student officer of the AIEE and Tau Beta Pi, and is a member of Phi Kappa Phi.

W. J. Giguere

❖

Arthur Gill (S'53–M'57–S'58) was born in Haifa, Israel, on April 18, 1930. He attended the Massachusetts Institute of Technology, Cambridge, Mass., where he received the B.S. and M.S. degrees in electrical engineering in 1955 and 1956, respectively. He received the Ph.D. degree in the same field from the University of California, Berkeley, in 1959.



A. Gill

From 1954 to1956 he served as a teaching assistant in the Department of Electrical Engineering at M.I.T. From 1956 to 1957 he worked in the research division of the Raytheon Manufacturing Company, Waltham, Mass., where he was engaged primarily in semiconductor circuitry design. Since 1957 he has been a member of the academic staff of the University of California, where he served first as a teaching associate in electrical engineering and now as an assistant professor. He is also associated with the Electronic Research Laboratory of the University, where he is working on information theory and automata problems, and with the advanced programming development group of the Bendix Computer Division of the Bendix Aviation Corporation.

Dr. Gill is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi, and the Association for Computing Machinery.

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Seymour Ginsburg (M'57), for a photograph and biography please see page 403 of the September, 1959 issue of these TRANSACTIONS.

Martin Graham was born on July 12, 1926, in New York, N. Y. He received the B.E.E. degree from the Polytechnic Institute of Brooklyn in 1947, the M.S. degree from Harvard University, Cambridge, Mass., in 1948, and the D.E.E. degree from Polytechnic Institute of Brooklyn in 1952. He served in the U. S. Navy as a radio technician from 1945 to 1947.

M. Graham

In 1951 he was granted a fellowship at Brookhaven National Laboratory, and remained there from 1952 to 1957 in the Instrumentation Division. Since 1957 he has been at The Rice Institute, Houston, Tex., where he is an associate professor of electrical engineering and director of the computer project. His present primary interests is in the design and construction of a large scientific digital computer.

Dr. Graham is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.

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James H. Jamison was born in Neptune, N. J., on October 28, 1928.

He joined the Bell Telephone Laboratories, Inc., Murray Hill, N. J., in 1953. He has worked on low-frequency transistor characterization, radio relay circuits, personal signaling communication receivers; and at present, he is engaged in the research and development of 160-megacycle bit rate circuits for pulse work.

J. H. Jamison

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Lloyd M. Lambert, Jr. (S'56–M'59) was born on May 10, 1929, in Olympia, Wash. He attended Stanford University, Stanford, Calif., in 1947, and received the B.S. degree from the U. S. Naval Academy, Annapolis, Md., and the M.S. degree from the University of California, Berkeley, in 1952 and 1958, respectively.

L. M. Lambert

From 1952 to 1956, he served in the U. S. Naval fleet, after

which he was placed on inactive duty in the Naval Reserve.

He was employed in 1957 by Sperry Gyroscope Company, Sunnyvale, Calif., on a transistor circuit studies project. During the first semester in 1957, he was engaged in circuit studies as a research assistant at the Electronics Research Laboratory of the University of California. He was an associate in electrical engineering at the University before he joined Aeronutronic Division of Ford Motor Company, Santa Ana, Calif., where he is presently engaged in work on the BIAX nondestructive readout element.

Mr. Lambert is a member of Sigma Xi.

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Harold M. Lucal (S'46–A'51–M'56) was born in Washington, D. C., on December 6, 1922. He received the B.S. degree in engineering physics from The Ohio State University, Columbus, Ohio, in 1944. After six months in aircraft antenna research and 20 months in the U. S. Navy, he returned to Ohio State, where he received the M.S. degree in electrical engineering in 1947. From 1947 to 1953 he was employed on the electrical engineering staff at Massachusetts Institute of Technology, Cambridge, Mass. He received the Sc.D. degree in electrical engineering at M.I.T. in 1953.

H. M. Lucal

Since 1953 he has served on the faculty of the University of Connecticut, Storrs, Conn., where he is now an associate professor of electrical engineering.

Dr. Lucal is a member of AIEE, the American Society for Engineering Education, Sigma Xi, Tau Beta Pi, Eta Kappa Nu, Sigma Pi Sigma, and Pi Mu Epsilon.

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Edward J. McCluskey, Jr., (S'51–M'55) was born in Brooklyn, N. Y., on October 16, 1929. He received the A.B. degree in mathematics and physics from Bowdoin College, Brunswick, Me. in 1953. He received the B.S., M.S., and Sc.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, Mass. in 1953 and 1956, respectively.

E. McCluskey, Jr.

From 1953 to 1955 he was a research assistant and instructor at M.I.T. In 1955, he joined the staff of Bell Telephone Laboratories, Whippany, N. J., where he did research in connection with electronic switching systems. He became associate professor of electrical engineering at Princeton University, Princeton, N. J., in September, 1959. Since 1956, he has been a lecturer at the College of the City of New York.

Dr. McCluskey is a member of Phi Beta Kappa, Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the Association for Computing Machinery.

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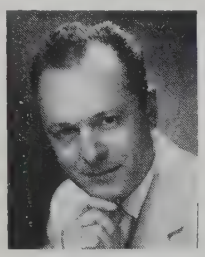
Arthur S. Melmed (A'56) was born on August 13, 1928, in New York, N. Y. He received the B.E.E. degree from the College of the City of New York in 1950 and the M.S.E.E. degree from Columbia University, New York, N. Y., in 1956.



A. S. Melmed

His experience includes two years of design and development of instrument servomechanisms while serving with the Signal Corps, and three years of design and development of analog computers at the Ford Instrument Co., New York, N. Y. Since 1956, he has been engaged in various phases of digital computer research at the AEC Computing and Applied Mathematics Center at New York University.

Mr. Melmed is a member of the ACM.

❖

G. L. Miller was born in New York, N. Y. on January 18, 1928. He was educated in England and received the B.S. degree in 1949, the M.S. degree in 1951, and the Ph.D. degree in 1957, all from the University of London.

He is currently a member of the Instrumentation Division of Brookhaven National Laboratory, Upton, N. Y., and his particular interests lie in the physics and application of devices. Dr. Miller is a member of the American Physical Society.

❖

Arthur G. Milnes (SM'58) was born in Heswall, England, on July 30, 1922. He received the B.S. degree in electrical engineering from the University of Bristol, England, in 1943 and the Master's degree in 1947. From 1948 to 1950 he carried out research work at the University on magnetic amplifiers, and in 1956 was awarded the D.Sc. degree for a book on this subject and other research papers.

A. G. Milnes

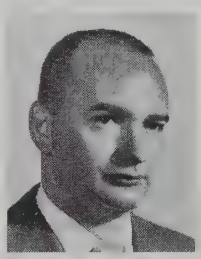
From 1943 to 1957 he was engaged in Scientific Officer posts at the Royal Aircraft Establishment, Farmborough, except for one year, 1954–1955, which was spent on a Royal Society-National Academy of Science Fellowship at Carnegie Institute of Technology, Pittsburgh, Pa.

Since 1957, Dr. Milnes has been an associate professor of electrical engineering at C.I.T. where he is studying the solid-state field.

Dr. Milnes is a member of the American Institute of Electrical Engineers, and of the Institution of Electrical Engineers (London).

❖

J. Crawford Noll (A'54–M'57–SM'57) was born in Trenton, N. J., on December 30, 1930. He received the B.S.M.E. and the M.S.M.E. degrees in 1952 and 1953, respectively, from the California Institute of Technology, Pasadena.



J. C. Noll

In July 1953, he joined the Bell Telephone Laboratories Inc., Murray Hill, N. J., as a member of the Transmission Systems Development Department and worked on development of circuits for a microwave radio system. Subsequently he has been concerned with transistorized radio equipment and transmission, and most recently, with circuits and transmission for a high-speed pulse-code-modulation system.

Mr. Noll is a member of Tau Beta Pi.

❖

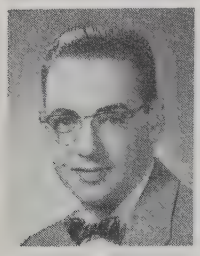
Howard R. Pate was born in London, Eng., on May 8, 1923. He reached Intermediate B.S. Eng. level at evening classes before being called to serve as a radar mechanic in the R.A.F. After World War II he became an assistant engineer in the Post Office Engineering Department Circuit Laboratory. After about sixteen years' experience on telephone work and nearly two years with the Plessey Company in England, he came to the United States in 1957. He is now an experimental engineer with the Instrumentation Division of Brookhaven National Laboratory, Upton, N. Y., where he has assisted in the development of the memory system and is currently in charge of the "debugging," maintenance, and further development program of the Merlin computer.

❖

Jerome S. Sallo was born in Chicago, Ill., on January 28, 1930. He received the B.S. degree in chemistry from the University of Illinois, Urbana, in 1951, and the M.S. and Ph.D. degrees in chemistry in 1952 and 1955, respectively, from the University of Chicago.

From 1955 to 1959 he was employed by the National Cash Register Company in Day-

ton, Ohio, where he engaged in research and development work in the field of electro-deposited magnetic materials. He is presently employed as a senior research scientist at the Research Center of the Minneapolis-Honeywell Regulator Company in Hopkins, Minn.



J. S. Sallo

Dr. Sallo is a member of the American Chemical Society, Sigma Chi, Phi Kappa Phi, and Phi Lambda Upsilon.

❖

Sidney J. Schwartz was born in Madison, Wis., on September 3, 1928. He received the B.S. degree in electrical engineering from the University of Wisconsin, Madison, in 1950.

S. J. Schwartz

After graduation he worked for the Wright Air Development Center, Dayton, Ohio, doing liaison work with several companies developing airborne computers. In 1951 he joined the Defense Engineering group at The National Cash Register Company in Dayton, and worked on electronic test equipment associated with airborne analog computers. In 1957 he transferred to the magnetic research group where he has been doing materials evaluation and application engineering on square-loop magnetic materials.

Mr. Schwartz is a member of Tau Beta Pi.

Robert T. Shevlin was born on August 30, 1932, in Brooklyn, N. Y. He has been attending New York University's Evening School of Engineering since 1954 and expects to receive the B.E.E. degree in June, 1960.

R. T. Shevlin

After four years in the United States Air Force (1950–1954), working on radar systems, he joined the engineering staff of the AEC Computing and Applied Mathematics Center at New York University, where he is now a senior engineer engaged in computer research and development. He is also a consultant to the Institute for Computer Research of the University of Chicago.

❖

Robert Spinrad was born in New York, N. Y. in March, 1932. He received the B.S. degree in engineering in 1953 and the M.S. degree in electrical engineering in 1954, both from Columbia University, New York, N. Y.

R. Spinrad

From 1954 to 1955 he was employed at the Bulova Research and Development Laboratories where he did developmental work in instrumentation and X-ray goniometry. In 1955 he joined the staff of the Brookhaven National Laboratory, Upton, N. Y., where he initially worked in the fields of nuclear instrumentation and medical electronics. Since 1957 he has been responsible for the design and development of Merlin, a large general-purpose digital computer.

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Stephen H. Unger (S'49–M'57), for a photograph and biography please see page 405 of the September, 1959 issue of these Transactions.

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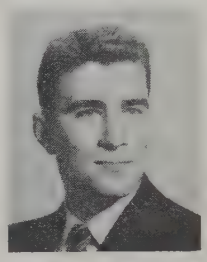
Eugene M. Zaitzeff (S'57–M'58) was born in Vladivostok, Russia, on December 5, 1929. He received the B.S. degree in 1957 and the M.S. degree in 1958, both in electrical engineering, from the University of Michigan, Ann Arbor.



E. M. Zaitzeff

From 1956 to 1958, he was a research assistant engaged in the design and construction of the MIC (Michigan Instructional Computer) and a teaching assistant in the electrical engineering department of the University of Michigan. In the summer of 1958, he acted as the technical interpreter for the University of Michigan Summer Computer Conference. He joined the staff of the Bendix Systems Division, Ann Arbor, Mich., in 1958, and has since been involved in analysis of pseudo-random noise generation methods and logical devices for optimum signal detection. His present responsibilities involve the integration of computational equipment into automatic communication links.

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Reviews of Books and Papers in the Computer Field

EDITED BY E. J. MCCLUSKEY, JR.†

Comments and suggestions on this new feature of IRE TRANSACTIONS ON ELECTRONIC COMPUTERS are solicited. Address them either to Professor McCluskey or to H. E. Tompkins, Editor.

The Cryosar—A New Low Temperature Computer Component—A. L. McWhorter and R. H. Rediker. (PROC. IRE, vol. 47, pp. 1207–1213; July, 1959.)

The cryosar is an interesting semiconductor device which deserves attention as a possible computer component. The principal new result reported in this paper is the discovery of a way of obtaining a breakdown voltage much larger than the sustaining voltage of the device. This results in a large negative resistance region reminiscent of the characteristic of a gas discharge. This effect is attributed to compensation in the P-type germanium crystals used. It is difficult to see how compensation could physically be responsible for this effect and, indeed, if one attempts to find empirical correlations for the ratio of the breakdown voltage to the sustaining voltage given in Table I of the paper, it is found that both the highest and the lowest ratio occurs for high compensation (matrix 37 and matrix 21, respectively), while the one essentially uncompensated matrix (49) shows an intermediate ratio.

A better correlation is found between this ratio and the net acceptor density ($N_A - N_D$). This also seems more reasonable physically since it would be expected that any barrier between the contacts and the bulk material would depend on the net acceptor density; the field in such a barrier region should determine the breakdown voltage rather than the field in the bulk material which should govern the sustaining voltage. The data given indicates that the sustaining field increases linearly with total impurity content ($N_A + N_D$). This is quite reasonable since the scattering mean free path of the current carriers will decrease with increasing ionized impurity density, thus requiring an increased sustaining field to insure that the ionizing mean free path remains shorter than the scattering mean free path.

Measurements of switching speed are reported indicating that under suitable conditions of overdrive and load, the cryosar can switch from the low conducting to the high conducting state in a few millimicroseconds. In this connection it should be pointed out that the cryosar is a high-impedance device in contrast to such devices as the Esaki diode and the cryotron. This means that in a switching network its useful switching speed will be limited by the shunt capacity of the load rather than the series inductance as is the case for the low-impedance devices mentioned.

If it is desired to keep the power dissipation to the order of a microwatt in order to achieve the high packing densities suggested in this paper, the current in the high conducting state must be about one microamp, since the sustaining voltage is of the order of one volt. Since it is difficult to imagine that the shunt capacity of any practical network load could be less than 1 $\mu\mu$f, the useful operating speed would be of the order of one megacycle. In order to increase this speed a higher power dissipation must be accepted, and for 100-mc operation a power dissipation per unit of 100 microwatts or more would be required. This means that the high packing densities suggested are not attainable simultaneously with the high speeds reported and some compromise must be reached which will depend on the minimum practical shunt capacity of a load network. In particular the 2×10^5 cryosars mentioned in the paper, if operated at 100-mc, might well require a helium refrigerator with a 20 to 100 hp compressor.

In comparison with other possible computer components, it should be pointed out that the thin film cryotron can run in the same speed and temperature range with an order of magnitude lower power dissipation and an appropriately higher packing density. The Esaki diode can also run in the same speed range with about an order of magnitude higher power dissipation but without the necessity of refrigeration.

It is reasonable to suppose that a great deal of technological development must yet be done on all three of the devices mentioned above before the practical limitations and relative advantages of each can be determined.

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A New Concept in Computing—R. L. Wigington. (PROC. IRE, vol. 47, pp. 516–523; April, 1959.)

The digital computing concept set forth here has as its basis a logical element which is simply a subharmonic generator. Power is applied at frequency f, and an output obtained at f/n which may of course have any one of n phases. An additional input signal is used to select one of these. The fundamental logical functions of *majority* and *negation* may be performed by such a circuit.

The author gives credit to John von Neumann for originating this idea and for recognizing its potential speed: if implemented at a microwave carrier frequency, digit rates of the order of 1000 megacycles seem attainable. There have been preliminary experiments along this line, in which variable-capacitance diodes are used as subharmonic generators, and the results have been reported elsewhere. It is useful to have a review of the basic idea as given here.

References are given, with little discussion, to the independent Japanese development of the same scheme. The emphasis in the Japanese work is on the potential simplicity of the logical element rather than on speed. Saturable-core reactors have been used as subharmonic generators, and, while work has been confined to kilocycle digit rates, it has been carried to the point of commercial application, while the microwave embodiment is still exploratory.

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Murray Hill, N. J.

Photoelectronic Circuit Applications—Sorab K. Ghandhi. (PROC. IRE, vol. 47, pp. 4–11; January, 1959.)

This paper describes some switching circuit applications of photoelectronic devices consisting of electroluminescent (EL) capacitors and photoconductive cells (PC) coupled together electrically and/or optically.

A brief description of some of the characteristics of the phosphors and photoconductors used precedes a qualitative discussion of the basic device which Dr. Ghandi has used in his experiments. As constructed, this device consists of layers of transparent conductor, EL phosphor and aquadag deposited on a microscope slide, plus a PC cell which views the EL capacitor through the slide. Since ac EL phosphors are used, the power is provided from an ac voltage source. The basic, series-connected device with electrical and optical coupling has two stable states. In the dark state, the PC resistance is very high, virtually all of the ac voltage appears across it, the EL cell remains dark, and the gain around the loop is less than unity. The device may be triggered to the "lighted" state, by application of an electrical trigger to the EL cell or an optical trigger to the PC. This trigger is chosen so that it carries the device to the point where the loop gain is greater than unity, switches, and then proceeds to the point where virtually all the ac source voltage appears across the EL cell as the light output increases and the cell resistance decreases.

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The dark-to-light switching time is fairly rapid (of the order of one millisecond) while the switching time from light-to-dark is very slow due to the very slow decay of conductivity characteristic of photoconductive cells which have high current amplification. Thus, it was found experimentally that a second or more was required for the conductivity to decay to a sufficiently low value to insure that the dark state would persist after removal of the trigger. Dr. Ghandi has studied a symmetrical bistable arrangement originally proposed by Tomlinson[1] which uses two opposed photoelectronic cells and utilizes regenerative gain in speeding up the light-to-dark switching time. This gain is applied in the manner used in the ordinary plate-coupled multivibrator. Dr. Ghandi found that light-to-dark switching times in this circuit were about two orders of magnitude more rapid than those obtained in the simple circuit. Thus, turn-off times compatible with turn-on times were obtained and cycle times were reduced to a few milliseconds. In addition, Dr. Ghandi presents experimental results on the operation of various combinations of the symmetrical bistable elements in circuits which perform the logical functions, AND, OR, and NEGATION, or act as pulse transmission circuits. The final part of the paper develops possible circuit configurations for the realization of a half-adder, a parity checker, and a shift register using these devices, but the circuits apparently have not been built and tested.

While the paper is clear and well written, it does not succeed in answering any question as to the possible utility of devices or circuits of this type in computer or instrumentation applications. Certainly, all of the ideas have been current for some time and are largely covered in the references cited by Dr. Ghandi. The device itself is in such an elementary state of development as to offer practically no information about the device characteristics which might result from a device engineering effort.

To be sure, detailed quantitative analysis of the device consisting of two highly nonlinear elements would be difficult, and hence the qualitative arguments used are justified. Nevertheless, some important points have been missed. For example, a simple block diagram connection representing the device can be drawn which points out significant features. Such a block diagram might consist, between input and output terminals, of a 40-db attenuator, a nonlinear current amplifier with a gain of 50 db, followed by a nonlinear low-pass filter with memory. In this block diagram, the attenuator represents the loss in the conversion of the electrical input signal to light in the *EL* phosphor (efficiency of *EL* phosphor is about 1 per cent) plus the optical coupling loss between the *EL* cell and *PC*. The current amplifier and the nonlinear low-pass filter with memory represent the current amplification and decay and turn-on characteristics of the *PC* cell.

In addition to pointing up the manifest difficulties in designing switching circuits with such a device the block diagram clearly indicates the essential role of good device engineering. It is well known that the rate of decay of *PC* cells varies inversely with their current amplification. Thus, in attempting to get useful device speeds it is important to design for best optical coupling between the *EL* and *PC* elements, since this reduces the coupling loss and hence the amplification required in the *PC*, and makes possible increased speed of operation. This writer estimates a coupling loss of at least 20 db for the device used by Mr. Ghandi in these experiments. Finally, it should be noted that many other characteristics of *EL* phosphors not mentioned in this article would have to be taken into account in assessing the usefulness of such devices. To mention a few, there are the variations in *EL* brightness with frequency, with phosphor aging and with temperature; the spectrum shift in *EL* emission (towards the blue) with increasing frequency; and various hysteresis effects.

Although this review has cited a number of difficulties that will not be easy to overcome, it still seems that the potential value of such devices may be very great. It should be possible to construct very large logical circuits including all necessary interconnections and gain elements by a series of evaporation operations. This should certainly result in an economical product. The first practical applications of circuits of this type known to the writer are now being made. Using these techniques, Hewlett Packard Corporation has developed a current amplifier with an amplification of 30. An array of these amplifiers is used in one of their instruments to drive a readout indicator. The entire amplifier array is fabricated as one part. These circuits differ from Dr. Ghandi's in that they use neon bulbs as light sources. This raises the question as to whether or not a neon bulb might be a more satisfactory light source than the *EL* phosphor.

Finally, Kilburn, Hoffman and Hayes[2] at the University of Manchester have done a very careful and excellent circuit and device engineering job on an *EL* curve plotter for digital computer print-out applications. The interested reader should refer to this article to gain a better understanding of the many device properties which must be taken into account in circuit designs using *EL* phosphor devices.

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[1] T. B. Tomlinson, "Principles of the light-amplifier and allied devices," *J. Brit. IRE*, vol. 17, pp. 141–154; 1957.

[2] T. Kilburn, G. R. Hoffman, and R. E. Hayes, "An accurate electroluminescent graphical-output unit for a digital computer," *Proc. IEE*, vol. 105, pt. B, pp. 136–144; March, 1958.

Design of Transistorized Circuits for Digital Computers—Abraham I. Pressman. (John F. Rider Inc., New York, N. Y., 1959. 310 pages +6 index pages +xi pages. Illus. 6×9. $9.95.)

Today the use of semiconductors in digital computer logic circuits is quite widespread, since it is seriously challenged only by magnetic and superconductive devices. It is, therefore, surprising that so little appears in available books on the detailed design of such circuits. Mr. Pressman's book gives, to my knowledge, by far the most comprehensive coverage on this subject to date.

The scope of this book can best be described by listing the chapter titles:

1) Basic Building Blocks in Digital Computers
2) Logical Chains in Digital Computers
3) Transistor Fundamentals
4) Transistor Transient Response
5) Diode Gating
6) Voltage-Switching Diode Gate Logic with Transistor Inverting Amplifiers
7) Current-Switching Diode Gate Logic with Transistor Inverting Amplifiers
8) Resistance Logic with Transistor Inverting Amplifiers
9) Direct-Coupled Transistor Logic
10) Miscellaneous Transistorized Logic Circuits
11) Design of Flip-Flops and Delay Multivibrators.

Detailed design calculations are given with the emphasis on worst-case design techniques so that the circuits will operate reliably with all variables at their extreme values in the sense of tending to make the circuits inoperative. Methods of calculating switching times are shown with numerous practical examples. The analysis has been done using simple piecewise linear approximations of the semiconductor device characteristics.

This book provides an excellent introduction to transistorized digital circuits for those with little detailed knowledge of transistor or computer circuitry and for those not yet converted to transistors for such applications. A more comprehensive use of references would have made the book even more useful to the beginner. Some aspects important to the selection and design of such circuits are treated very lightly or not at all. Among these are the considerations of noise margin, diode reverse recovery effects, and relative comparisons of the various types of circuits on the basis of cost, power dissipation, tolerances, speed, etc.

In general, Mr. Pressman's book is a welcome addition to the literature. It should prove quite useful to circuit designers in the computer field.

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Whippany, N. J.

Shifting Counters—C. Eldert, H. J. Gray, Jr., H. M. Gurk, and Morris Rubinoff. [*Commun. and Electronics*, no. 35 (*Trans. AIEE*, vol. 77, pt. I), pp. 70–74; March, 1958.]

Analysis of Shift Register Counters—Frederick H. Young. (*J. Assoc. Comp. Mach.*, vol. 5, pp. 385–388, October, 1958.)

Can you arrange N binary digits on a circle and rotate them once past an n bit window (register), with no repetitions among the N words appearing in the window? Whatever your answer, you may

still find both articles interesting and instructive. For certain value of n and N, the digit cycles exist and the next value (0 or 1) to be shifted into the register when a "count" or "step" signal occurs may be obtained from a list in a memory (see Eldert *et al.*), or may be generated by a simple logic circuit (see Young).

Eldert, Gray, Gurk, and Rubinoff's presentation of the "shifting counter" is embedded in an interesting and rather general discussion of counters. They discuss the program counter in a special purpose digital computer employing dynamic (SEAC-type) circuitry. The address of the next instruction appears in a shift register; the next bit to be entered into this register is stored in memory and obtained whenever an instruction is read. Instead of storing the next bit values, these could be generated by wired logic; the authors give logical equations for this type of design for a number of cycle lengths. They also discuss the construction of cycles and some mathematical properties of cycles.

Young sheds some light on the lengths of possible cycles when the value of the bit to be inserted is the sum, modulo 2, of the bit to be shifted out and some other bit in the register. A full cycle of 2^n steps or words is not possible with this generator which partitions the 2^n words into mutually exclusive cycles, one of which has length 1 (the word composed of all zeros). Young tabulates all possible cycle lengths, using the sum-modulo-2-generator, for $n=2$ to 7 inclusive, and gives relations that must be satisfied if a particular cycle length exists for arbitrary n. Logical designers with less mathematical background will surely find the theorems, if not the proofs, interesting and potentially useful.

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Matrix Analysis of Logical Networks—E. J. Schubert. [*Commun. and Electronics*, no. 35 (Trans. AIEE, pt. 1, vol. 77), pp. 10–13; March, 1958.]

This paper presents a method for analyzing gate networks (combinational logic circuits). Each variable in the network (input variable, or output of one of the gates) is represented by a row-vector f having 2^p components where p is the number of input variables. Each component F_i of this vector f corresponds to one row of the table of combinations, and $F_i=1$ if the corresponding variable is equal to one for the ith row of the table of combinations and is equal to zero otherwise. Thus, the F_i are identical with the coefficients in the canonical expansion of the variable represented by f. Rules are given for computing the f vector corresponding to the product or sum of two variables directly from the f vector representing the variables, and also for writing down directly the f vector representing the output of an AND gate whose inputs are all circuit inputs. An example is given of the use of the f vectors to analyze and simplify a gate network.

While the techniques presented in this paper may be useful when analysis is carried out on a digital computer, it is difficult to agree with the author's claim that for hand calculation the f matrices have a significant advantage over "conventional" methods or even that the f matrices represent a novel method of analysis.

The author's example is one which can actually be handled more simply by standard Boolean algebra techniques. The problem is to simplify:

$$Y_2 = (X_2 + X_3' + X_5' + X_6 + X_7 + X_8')(X_2X_3'X_5X_6X_8')$$

and

$$Y_4 = X_1'X_2X_3X_4'X_5X_7Y_2'.$$

Since $(A+C)(AB)=AB$, Y_2 can be written as $Y_2=X_2X_3'X_5X_6X_8'$. Then $Y_2'=(X_2'+X_3+X_5'+X_6'+X_8)$, so that

$$Y_4 = (X_1'X_2X_3X_4'X_5X_7)(X_2' + X_3 + X_5' + X_6' + X_8)$$

or $Y_4=X_1'X_2X_3X_4'X_5X_7$. These are the simplifications obtained by the author.

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Transition Matrices of Sequential Machines—S. Seshu, R. E. Miller, and G. Metz. (IRE Trans. on Circuit Theory, vol. CT-6, pp. 5–12; March, 1959.)

The authors discuss sequential machines in the sense of E.F. Moore; *i.e.*, for each state and each input, a) a next state occurs, and b) an output occurs which depends only on the present state. For each input i, the transition matrix T^1 is defined as that matrix whose jkth entry is a one if state q_j goes to state q_k under input i, and zero otherwise. Several properties of transitions matrices which are invariant under multiplication by transition matrices are proved. Two types of "equivalences" between sets of states are defined. A reduction procedure for machines based on transition matrices and equivalent states is then given. However the entire process of reduction of Moore machines by transition matrices only is not accomplished. For, while the testing of sets of states for equivalence is effected by transition matrices, the determination of those sets to be tested is not.

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Hazards and Delays in Asynchronous Sequential Switching Circuits—S. H. Unger. (IRE Trans. on Circuit Theory, vol. CT-6, pp. 12–25; March, 1959.)

It is well known that electronic asynchronous circuits are rather sickly specimens when exposed to the full gambit of diseases which arise from variations in the response times of active elements and variations in the propagation times of signals between active elements. It is so much easier to design reliable clocked circuits that unclocked ones (unclocked = asynchronous) are notable by their rarity nowadays.

There are two principal schools of thought among those who are striving to overcome this difficulty, and thus benefit from the (in principle) faster computing rates which may be achieved by abandoning clocked control. One school, represented by D. E. Muller of the University of Illinois, advocates the design of "speed independent" circuits, *i.e.*, circuits which will give correct performance regardless of the operating speeds of the elements of which they are composed. The other school of thought, represented by the followers of D. A. Huffman, seeks understanding of timing troubles within the framework of Huffman's theory of asynchronous circuits, a theory which, in its original form, is adequate for the design of relay circuits but fails to mirror nature where the magnitude of stray delays approaches the operating times of the active elements.

The present paper is written in the latter vein. The author introduces the notion of an *essential hazard*, which is identified with a flow table pattern in which three successive changes of a single binary input variable leads to a different final state from that resulting from a single change of the variable. He demonstrates that in the absence of essential hazards, the flow table may be safely realized without the insertion of special safeguarding delays, regardless of the nature of the stray delays in the circuit. On the other hand, he shows in a lengthy proof that if an essential hazard is present, there will always exist a particular configuration of stray delays which will cause a circuit realizing the flow table to function incorrectly unless special safeguarding delay is added. Finally, his third principal contribution is a demonstration that any flow table containing any number of essential hazards may be realized safely by a circuit containing but a single such added delay element.

Unger's results are significant and are obtained by ingenious means. Lovers of rigor will be disappointed that he introduces a number of crucial ideas (*e.g.*, *proper circuit, inertial delay*) by means of rather vague definitions, but vigor is present in abundance.

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A Note on Memory Aspects of Sequence Transducers—J. M. Simon. (IRE Trans. on Circuit Theory, vol. CT-6, pp. 26–29; March, 1959.)

Three classes of pulse-type, synchronous, sequential transducers are considered in this paper. These can be characterized as follows: the present output is a function of 1) the present input and a finite number m of past inputs, 2) the present input and a finite number n

of past outputs, or 3) the present input and a finite number m of past inputs and a finite number n of past outputs.

Consider class 1). An end state is determined for any length m input sequence. At least one input sequence of length m will place the (reduced) transducer in a unique state. If the next output following at least one such length m input sequence is dependent upon the next input, then the transducer is said to have "memory of length m." More generally, whether there is this dependence or not, the transducer is said to have "memory of maximal length m." Three general theorems are proved concerning class 1) transducers. The first concerns a necessary and sufficient condition that a transducer have a memory of maximal length m, the second concerns a necessary condition that a transducer have a memory of length m, and the third places an upper bound on the number of distinguishable states for a (strongly connected) transducer with a memory of length m. Analogous definitions and theorems are given for the class 2) transducers, and the class 3) transducers are discussed briefly.

This paper may be regarded as a contribution to the "gedanken" literature on finite machines. However, for the practicing logical designer, there is nothing useful here. No synthesis techniques are given, and the few comments on realization are self-evident once the definitions are understood.

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Murray Hill, N. J.

Equivalent Sequential Circuits—W. J. Cadden. (IRE Trans. on Circuit Theory, vol. CT-6, pp. 30–34; March, 1959.)

The problem considered is that of classifying various modes of operation of sequential switching circuits, and of determining when circuits operating in various modes are essentially equivalent.

Cadden considers the following cases:

1) Both input and output signals in the form of pulses (PP).
2) Input signals in the form of pulses; output signals in the form of levels (PL).
3) Both input and output in the form of levels (LL).

Two circuits operating in different modes are termed equivalent if the same sequence of input states applied to each circuit yields the same sequences of output states. In the case of LL circuits it is meaningless to speak of input sequences in which consecutive input states are the same; therefore, such sequences are excluded when comparing LL circuits to either of the other two types.

A procedure is given for transforming state tables defining PP circuits into state tables defining equivalent PL circuits. Other procedures are given for PL to PP and LL to PP transformations. In connection with the PP to PL transformation, Cadden points out that this process can also be used to convert a PP circuit into another PP circuit whose behavior differs from that of the original circuit in that each output signal will be delayed by one unit of time.

The paper, which is clearly written and concise, is a useful contribution to the literature in that it clarifies the relationships among an important class of circuits, and introduces some useful terminology. A similar study, broadened to include various types of synchronous and asynchronous sequential circuits, would be most welcome.

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Whippany, N. J.

The Theory of Autonomous Linear Sequential Networks—Bernard Elspas. (IRE Trans. on Circuit Theory, vol. CT-6, pp. 45–60; March, 1959.)

Over the past several years considerable work has been done in extending and generalizing the concept of a linear sequential network, initially proposed by D. A. Huffman. In particular, many authors have recently concerned themselves with systems other than binary. The motivation for much of this work has come to a large extent from applications in communications systems; *e.g.*, generation of "pseudo-random" sequences of digits, and coding and decoding problems.

As the title implies, this paper concerns itself with the analysis and synthesis of certain types of linear sequential networks. The author restricts himself to the autonomous (unexcited) behavior of modulo-p (p a prime) nonsingular networks. Within these restrictions this paper is probably the most complete, although by no means the only treatment of this subject which has appeared to date.

The author defines linear sequential networks as arbitrary interconnections of unit-delay elements, modulo-p adders, and integral-valued constant gain elements (also mod-p). These, then, constitute a special class of synchronous sequential machines whose autonomous behavior is describable by the matrix equation

$$X' = TX$$

where X is a column matrix representing the present state of the network, X' is a column matrix representing the next state of the network, and the square matrix T prescribes the transition between the two. (In the literature the terms *transition* and *characteristic* matrix have been applied to T.) All elements of X, X' and T are integers, mod-p. Attention is restricted to networks (nonsingular) for which T has a unique inverse, in which case the sequences of states are shown to be periodic.

As in the case of ordinary linear autonomous systems, the behavior of these networks is determined essentially by a certain polynomial, $\phi(x)$, the characteristic polynomial of the T-matrix. The majority of the paper is devoted to the analysis problem, determination of the cyclic structure of the state diagram. Analysis is performed by examination of the characteristic polynomial and, when necessary, the T matrix itself. The cyclic structure is summarized by "cycle sets" which are enumerations of the periods of the various state cycles. It is shown that a single cycle of maximal-length period is generated when $\phi(x)$ is one of a certain class of irreducible polynomials. A complete discussion of networks having irreducible characteristic polynomials is given. The case of factorable $\phi(x)$ is treated by defining products of cycle sets. The treatment is concise and complete in the case where $\phi(x)$ has distinct factors, but necessarily becomes quite complex in the case of repeated factors. In this latter case, the cyclic behavior of the network may become quite involved and is not in general completely determined by the characteristic polynomial alone.

The synthesis problem is considered in two parts: 1) the determination of an appropriate $\phi(x)$ for a given cycle structure, and 2) the realization of a network from a given $\phi(x)$. One might compare with 1) the approximation problem in modern network synthesis and 2) the problem of realization of a given rational network function.

The second step is accomplished by selecting a canonical form of the T-matrix (a direct sum of submatrices in companion form) which is realizable by a set of isolated feedback shift registers; that is, shift registers with feedback to the first stage. The first step is accomplished in a more or less trial-and-error fashion. The desired cycle set is decomposed into the product of several "canonical cycle sets," the latter being the cycle sets generated by feedback shift registers. A difficulty here is that one must have available a tabulation of all of all of the pertinent canonical cycle sets to use as trial divisors. As one might suspect, not all cycle sets are realizable. Therefore, some necessary conditions for cycle set realizability are given. However no sufficient conditions except the decomposition procedure itself have been derived. The synthesis procedure takes on a more manageable form when the author applies it to single cycles rather than to complete sets.

In an appendix some theorems from the theory of Galois fields are stated to indicate relations between irreducible characteristic polynomials and cycle periods. The paper also discusses relations to Huffman's D operator, and network synthesis using trigger flip-flops to replace delay elements.

Although the author states that he is primarily interested in economical synthesis procedures, the paper's chief value, in this reviewer's opinion, lies in its comprehensive analysis of the cyclic behavior of linear sequential networks. Much of the material presented has been derived independently by others. However, this paper, especially in its treatment of the case of factorable characteristic polynomials, appears to be the most detailed study so far.

A minor criticism: Galois theory has been relegated to an appendix although it actually forms the foundation for much of the work. Many of the results could have been deduced directly from Galois theory if use had been made of an isomorphism which exists between powers of a matrix with irreducible minimum equation and the elements of a multiplication group of a Galois field. It is quite likely that a more coherent and unified development would have resulted from recognition of this isomorphism.

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Abstracts of Current Computer Literature

(THROUGH JULY, 1959)

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Comments on this abstract service are welcomed. Please let us know if it is useful to you, or if it could be improved.

—The Editor.

A-1: EQUIPMENT—THEORETICAL DESIGN

406
Indexing and Control-Word Techniques, by G. A. Blaauw (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 288–301; July, 1959.

In large-scale computers the details of data handling, such as indexing, transmission and ordering, may be performed either by programming or by built-in machine operations. An analysis of the most frequently performed functions justifies the expansion of single-valued index quantities to three-valued control words and the specification of built-in increment, count and refill operations to be used with these control words. STRETCH, the large-scale computer which is being developed by IBM for the Los Alamos Scientific Laboratory, provides these control-word functions for data-handling operations.

A-2: EQUIPMENT—COMPONENTS AND CIRCUITS

407
P-N-π-N Triode Switching Applications, by V. H. Grinich and I. Haas (Fairchild Semiconductor Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 108–113; June, 1959.

The characteristics and switching applications of a developmental diffused silicon p-n-π-n triode capable of handling short pulses of current of the order of 100 amperes are discussed. The unit consists of a low and high conductivity region (over 500 megohms and less than 1 ohm, respectively) with an intermediate negative resistance region. The characteristics can be controlled by the base lead, which makes it a flexible device for applications in the computer and communications fields. Experimental data covering current handling capabilities, frequency limitations, and switching times are presented in conjunction with representative circuits. Two particular circuits discussed are an 80-ampere, 500-mμsec pulse generator with rise and fall times in the order of 150 mμsec and 300 mμsec, respectively, that can operate up to a kilocycle repetition rate; and a 4-ampere, 60-mμsec pulse generator with a PRF of 100 kc. Other examples described include monostable, bistable, and astable circuits.

408
Integrated Devices Using Direct-Coupled Unipolar Transistor Logic, by J. T. Wallmark and S. M. Marcus (Radio Corp. of America); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 98–107; June, 1959.

A new logic system which uses direct-coupled unipolar transistors is analyzed. Semiconductor devices of extreme miniaturization, built by an integrated device design, which use this logic system are described and the integration of passive system components into the devices is discussed. It is shown that unipolar transistors have important advantages over bipolar transistors in speed, tolerance of stray signals and noise, and device miniaturization.

409
Thin Film Magnetization Analysis, by K. Chu and J. R. Singer (University of California); PROC. IRE, vol. 47, pp. 1237–1244; July, 1959.

The use of a graphical method for analyzing the magnetization direction of ferromagnetic thin films in terms of the magnetic energy and for predicting the hysteresis loop shape is discussed. Three major magnetization conditions of importance in computer applications are considered: 1) condition of magnetization with a 180° field applied; 2) condition of magnetization with a 90° field applied; and 3) condition of magnetization with both the 90° and the 180° fields applied. The hysteresis loop shapes corresponding to these magnetization conditions are predicted and constructed. The results show close identity to those observed experimentally.

410
Superconducting Computer Elements, by E. H. Rhoderick (Services Electronics Res. Lab.); *Brit. J. Appl. Phys.*, vol. 10, pp. 193–198; May, 1959.

The present status of superconducting circuit components, including both active elements of the "cryotron" type and passive elements such as persistent current memory cells, is discussed. The factors which affect the speed of operation of these devices are pointed out, and the future is shown to be closely linked with developments in the technology of thin metallic films.

411
The Cryosar—A New Low-Temperature Computer Component, by A. L. McWhorter and R. H. Rediker (M.I.T. Lincoln Lab.); PROC. IRE, vol. 47, pp. 1207–1213; July, 1959.

The cryosar, a high-speed two-terminal computer component whose operation (at liquid helium temperature) is based on impact ionization of impurities in germanium, is described. Two types of cryosars are discussed: the first, fabricated using uncompensated germanium, exhibits a high resistivity ($\sim 10^7$ ohm-cm) until a critical field ($\sim$10 volts/cm) is reached, after which the current increases by as much as seven orders of magnitude; the second, fabricated using compensated p-type germanium, has similar electrical characteristics except that a negative resistance region occurs between the high- and low-impedance states, making bistable operation possible. These properties are due to bulk effects, and since both contacts are ohmic, the device is bilateral. The first type of cryosar can perform the functions of an ordinary diode; the bistable cryosar can be used as a memory element, multivibrator, or flip-flop. Both types are very fast, the speed being limited by the turn-on time of 10^{-8} seconds or less. Since the active region of each cryosar is limited to the volume directly between its two contacts, a large number of independent cryosars may be placed on one wafer of germanium. Present results point to excellent reliability and reproducibility of the individual elements, making feasible the plating or evaporation of large arrays, possibly integrated into microprinted circuits. If one requires the cryosars alone, it should be possible to fit 200,000 into a cubic inch.

412
The Transpolarizer: An Electrostatically Controlled Circuit Impedance with Stored Setting, by C. F. Pulvari (Catholic University of America); PROC. IRE, vol. 47, pp. 1117–1123; June, 1959.

A new device which operates by the controlled transfer of polarization through two or more ferroelectric dielectric sections in series and is therefore named "transpolarizer" is discussed. This device represents a new basic means for storing and gating electrical signals and, in general, means to control circuit impedance in any predetermined manner according to a stored setting. The operation of a two-section transpolarizer is described. The unique storage, switching, and control properties of the transpolarizer open a large field of new applications and permit production of new devices and systems such as: recording and reproducing of intelligence in general and, more particularly, switching with a permanent setting, small- and large-scale storage devices with nondestructive readout, decoders, function generators, etc.

413
Photoelectronic Circuit Applications, by S. K. Ghandhi (General Electric Co.); PROC. IRE, vol. 47, pp. 4–11; January, 1959.

A study of the properties of electroluminescent cells and photoconductors, and of the applications of these elements to the design of switching circuits is presented. The asymmetrical bistable stage is taken up in detail and analyzed with a view to determining its advantages and disadvantages. It is shown that this stage suffers from the inherent disadvantage that any improvement in the speed of turn-on results in a deterioration of the recovery characteristic. Furthermore, the switching requirements for turn-on and turn-off are dissimilar. A symmetrical version of this circuit is also presented; this circuit eliminates many of the disadvantages of the asymmetrical version, and also speeds up the recovery characteristic considerably without increasing the turn-on time. Circuits for performing the logical operations of transmission, negation, conjunction, and disjunction are developed and their principles of operation are described. In conclusion, techniques for the synthesis of over-all computing operations, such as those of a half-adder, even parity checker, and a shift register, are developed.

414
Asynchronous Electronic Switching Circuits, by M. Kliman and O. Lowenschuss (Sperry Rand Corp.); 1959 IRE NATIONAL CONVENTION RECORD, pt. 4, pp. 267–274.

A study of asynchronous electronic switching circuits is discussed, using and extending concepts introduced by Huffman, Caldwell, and Unger. Circuits in this class operate without using a master-clock oscillator, multivibrator timing chains, or synchronizing pulses. Signals are represented by

variables which can assume one of two levels, and are propagated through individual elements at a speed determined solely by that element. Advantages of these circuits are that they provide a speed increase greater than the equipment increase, and that they enhance reliability. Experiments using standard resistance-coupled transistor circuitry have verified the design procedures, and have resulted in an appreciable speed increase over the standard use of the same circuits.

415
Fast Microwave Logic Circuits, by D. J. Blattner and F. Sterzer (Radio Corp. of America); 1959 IRE NATIONAL CONVENTION RECORD, pt. 4, pp. 252–258.

Basic AND and NOT logic circuits which can operate with RF pulses of less than two millimicroseconds duration at a carrier frequency of 3000 mc and half-adders which utilize these elements are described. The circuits are constructed with strip line printed circuit techniques and point contact semiconductor diodes. Unlike other carrier approaches, these circuits keep the information in RF form through all steps of the logic operations; *i.e.*, both inputs and outputs of all elements are RF pulses. It is pointed out that the proper amplification for these passive logic elements can be provided by parametric subharmonic oscillators which utilize the variable reactance of a germanium point contact diode.

A-3: EQUIPMENT—SUBSYSTEMS

416
Magnetic Core Logic in a High-Speed Card-to-Tape Converter, by E. Block and R. C. Paulsen (IBM Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 169–181; June, 1959.

A static magnetic shift circuit and the logical connectives derived from it are described. The prime advantages of magnetic circuits are their low cost, high reliability, and ease of maintenance. The application of these circuits to the design of a card-to-tape converter is discussed.

417
Magnetic Core Matrices for Logical Functions, by A. L. Freedman (Ericsson Telephones Ltd.); *Electronic Eng.*, vol. 31, pp. 358–361; June, 1959.

The general principle of a method for performing logical functions using matrices of magnetic cores having a square hysteresis loop is explained and some applications are discussed. The field of usefulness of the method is outlined and its inherent advantages and limitations are pointed out.

418
An Electro-Optical Shift Register, by T. E. Bray (General Electric Co.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 113–117; June, 1959.

An electro-optical shift register composed only of electroluminescent and photoconductive cells is discussed. While its measured operating speed probably does not make this shift register currently competitive in high-speed applications, it is amenable to construction in an extremely small volume, and has certain other unique characteristics.

419
Thin Ferromagnetic Films, by A. C. Moore; *RRE J.*, no. 43, pp. 61–88; April, 1959.

An account of the work at the Royal Radar Establishment on the preparation and properties of thin ferromagnetic films is presented. The work provides the prospect of a computer store in which a million bits would occupy less than an eighteen-inch cube, and which would possess a switching time faster than twenty millimicroseconds. The store would be cheap and easily constructed.

420
Thin-Film Memories, by E. E. Bittman (Burroughs Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 92–97; June, 1959.

A small random-access memory which uses deposited magnetic thin films as storage elements and which has a cycle time of one microsecond is described. Information is read from or written into the memory by linear or word selection techniques. The addressing, driving, and sensing circuits are transistorized. The deposited thin films are 2000 Å thick, switch in 0.1 μsec and generate a 5-mv output signal in the sense winding. A sense signal of opposite polarity from a selected element is obtained when a "1" or a "0" is read out. A memory-plane wiring configuration which is least susceptible to noise has been selected.

421
Magnetic Drum Time Compression Recorder, by W. R. Chynoweth (General Electric Co.); 1959 IRE NATIONAL CONVENTION RECORD, pt. 4, pp. 242–251.

A magnetic drum time compression recorder which has a time compression ratio of 82,800:1 and is capable of a record-playback bandwidth of 100 kc to 7.5 mc, using either pulse bias or dc bias recording, is described. Air-bearing techniques are used to support the record and playback heads within 200 microinches from the drum surface, which is sufficiently close to resolve a 0.001-inch recorded wavelength. The frequency response is flat within ±2 db over the operating bandwidth. At a 30 ma record level, the signal-to-full-bandwidth-rms-noise is 20 db. Present indications are that the life of the drum surface and the heads is indefinitely long when they are properly adjusted.

422
The Recording and Reproduction of Signals on Magnetic Medium Using Saturation-Type Recording, by J. J. Miyata (National Cash Register Co.) and R. R. Hartel (Clevite Electronic Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 159–169; June, 1959.

The various factors affecting the resolution in saturation magnetic recording are considered. The effect on the recording process of the B-H characteristics of the coating thickness, record-head gap width, head-to-coating separation, self-demagnetization, and record-head residual magnetization are discussed. Equations for the playback process relating the signal amplitude and pulse width to the coating thickness, head-coating separation, and effective gap width of the playback head are derived. It is shown that the greatest improvement in resolution can be obtained by the development of an extremely thin coating with high ratio of coercitivity to remanence and having a rectangular B-H loop. The extremely thin coating will reduce the shortcomings of the record-head field pattern, the self-demagnetization effect, and the loss of resolution in the playback process.

423
A Design for an Automatic Graph Plotter, by M. P. Atkinson and D. L. A. Barber (National Physical Lab., England); *Proc. IEE*, vol. 106, pt. B, pp. 299–306; May, 1959.

A design for an automatic graph plotter using digital techniques throughout and incorporating full scaling and zero-shift facilities is described. Alternative approaches to some sections of the design are discussed. The equipment makes use of transistors and printed circuits for both arithmetic and logical operations and incorporates a mechanical design for the table movements which makes possible the use of small low-powered driving motors with a high rate of acceleration. With a suitable input device, points close together can be plotted at the rate of three per second with a positional accuracy better than 0.01 inch.

424
NORC High-Speed Printer, by G. H. Cleissner (U. S. Naval Proving Ground); *Commun. Assoc. Comp. Mach.*, vol. 2, p. 25; June, 1959.

The NORC high-speed printer, whose main components are a Charactron shaped beam cathode-ray tube and two 35-mm cameras, is briefly described. The machine can be programmed to generate simple line drawings.

425
Circle Networks of Probabilistic Transducers, by M. Kochen (IBM Corp.); *Information and Control*, vol. 2, pp. 168–182; June, 1959.

A circle of devices, each characterized by a one-bit output which is statistically correlated with the outputs of its right and/or left neighbor at the preceding time period, is considered. It is shown that, provided no input-output relation is deterministic, this system will eventually become completley disorganized in the sense that it will behave like a collection of independent parts with completely unpredictable behavior. The rate at which this disorganization occurs under various conditions is calculated. A concrete version of this model is a sequential circuit of imperfect relays. A possible application to the determination of certain reliability

parameters is given. The relation to a similar model for statistical mechanics by Kac is shown.

426
Uniform Cooling Air Flow During Computer Maintenance and Operation, by A. Perlmutter (Sylvania Electric Products, Inc.); 1959 IRE NATIONAL CONVENTION RECORD, pt. 6, pp. 148–157.

The use of direct air cooling with a positive pressure system to maintain a uniform cooling air flow during maintenance and operation of the tube-type UDOFT (Universal Digital Operational Flight Trainer) computer is discussed.

A-4: EQUIPMENT—DIGITAL COMPUTERS

427
On Economical Debugging, by C. R. Blair (Dept. of Defense); *Computers and Automation*, vol. 8, p. 15; May, 1959.

A suggestion is made to retain the desirable features of direct console debugging without the attendant waste of valuable machine time by having a duplicate set of input-output equipment coupled with low-speed storage. The machine may continue on an operational problem, while the programmer works with the slow-motion equipment at a cost comparable with external "debugging."

A-5: EQUIPMENT—ANALOG COMPUTERS

428
A High-Speed Analog-Digital Computer for Simulation, by R. C. Lee and F. B. Cox (M.I.T.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 186–196; June, 1959.

The principles of operation and logical design of an analog-digital computer capable of simulating complex physical systems in real time are described. Information in the machine is represented by an analog voltage pulse and a digital number. Arithmetic operations are performed in time-shared analog computing components and conventional digital logical elements. A novel floating-point arithmetic feature is provided to extend the dynamic range of the machine variables. Instructions and constants are stored on a magnetic drum before computation begins. The instructions determine the sequence of computer operations, and both the instructions and the constants are arranged so that random access to the drum is not needed. The programming techniques developed for the computer are described. The inherent simplicity of these techniques should permit engineers directly concerned with simulation to program their own problems for computer solution.

429
Digital-Analog Function Generators, by R. W. Hofheimer and K. E. Perry (M.I.T. Lincoln Lab.); *U. S. Government Res. Repts.*, vol. 31, p. 459(A); June 12, 1959. PB 139 210 (Order from LC, Mi $2.40 Ph $3.30).[1]

Digital-analog function generators are discussed. They are similar in application to digital-to-analog converters except that their outputs, instead of being proportional to the inputs, are proportional to functions of the inputs. If, for example, the input to a digital-analog function generator is x in digital form, then the output can be an analog voltage proportional to $\sin x$ or $\log x$ or any of a wide variety of functions of x. Functions of more than one input variable can also be handled.

430
The Design of Biased Diode Function Generators, by C. C. Ritchie and R. W. Young (Brunel College of Tech.); *Electronic Engrg.*, vol. 31, pp. 347–351; June, 1959.

The design of biased diode function generators is discussed. Equations relating the number of diode sections, the minimum error obtainable, and the spacing of the diode section to give this minimum error are derived. The design of a sine function generator which uses silicon diodes as switching elements is covered.

431
Rotating-Disk Function Generator for Analog Computers, by M. E. Young, W. M. Alexander, and H. D. Schwetman (Baylor University); *Rev. Sci. Instr.*, vol. 30, pp. 318–322; May, 1959.

A simple device for the production of varying potentials which represent four functions of the form $f(t)=at$, $f(t)=at+b \sin \omega t$, $f(t)=at^2+b$, and $f(t)=a$ for 50 msec $\leq t \leq$ 100 msec and a rate of operation of 5 cps is described. The device makes use of a rotating disk of variable radius to control the light incident upon the cathode of a photomultiplier tube. The accuracy of the functions is about 4 per cent with the exception that maximum errors of 4 to 10 per cent are observed near points of discontinuity. The method of preparing the disk, use of the functions in the solution of linear, ordinary differential equations, and an analysis of the error are presented.

432
A Four-Quadrant Multiplier Using Triangular Waves, Diodes, Resistors, and Operational Amplifiers, by P. E. Pfeiffer (Rice Institute); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 222–227; June, 1959.

A simple scheme of switching triangular waves and measuring the average current through resistors into a low impedance summing point which makes possible four-quadrant multiplication with four diodes, precisely adjusted resistors, and a means of measuring the current, is described. A practical circuit utilizes one operational amplifier to obtain $-(X+Y)/2$ and a second such unit to measure the summing point current. Addition of four auxiliary diodes reduces circuit interactions and makes less stringent requirements on the diodes. A simple operational adjustment procedure is described. Also, a simple means for obtaining the precise resistance balance is outlined. Calibration does not depend upon triangular wave frequency or symmetry. The amplifiers are not required to handle the triangular wave frequencies.

433
A Negative Resistance for DC Computers, by P. V. Indiresan (University of Birmingham); *J. Brit. IRE*, vol. 19, pp. 401–410; July, 1959.

A dc negative resistance suitable for use in analog computers is described. The circuit uses two transistors and eight resistances and is compensated against unbalance in the two transistors. A nomogram has been constructed to simplify the design of the circuit for any required values of negative resistance. The properties of, and the differences between, series and shunt type of negative resistances are discussed. The circuit described gives a shunt type of negative resistance.

B-1: SYSTEMS—THEORETICAL DESIGN

434
Reliability of a Physical System, by H. Mine (Defense Academy, Yokosuka, Japan); SPECIAL SUPPLEMENT TO IRE TRANS. ON CIRCUIT THEORY AND ON INFORMATION THEORY, vol. CT-6 and vol. IT-5, pp. 138–151; May, 1959.

The general concept of the reliability of the complex physical system which consists of a number of unreliable elements is presented. Such a system is analyzed systematically by means of algebraic and topological theory. Various properties concerning the system reliability are established. The methods of linear graph theory are used to find the theoretical relationship between element reliability and system complexity. Optimization of the reliability of a basic system under certain constraints can be accomplished by the application of the theory described. A numerical procedure for finding the optimum solution is developed to facilitate computation.

435
Increasing Reliability by the Use of Redundant Machines, by D. E. Rosenheim (IBM Watson Lab.) and R. B. Ash (Columbia University); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 125–130; June, 1959.

The improvement of reliability and availability through redundancy of entire machines rather than of components is investigated. An attempt is made to break down the cost of operating a digital computer and to determine the relationship between cost and system failure. Three specific cases are

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If LC is indicated, write to: Library of Congress, Photoduplication Service, Publications Board Project, Washington 25, D. C. Make check or money order payable to: Chief, Photoduplication Service, Library of Congress.

If OTS is indicated, write to: Office of Technical Services, U. S. Department of Commerce, Washington 25, D. C., or to any Department of Commerce field office. Make check or money order payable to: OTS, Department of Commerce.

discussed. Case 1—When n machines are operated independently, processing the same input data. The output is taken from a single one of them; if this machine fails, the output is promptly switched to a machine which is operating properly. As soon as repairs can be completed, the machine which had failed is returned to operation. System failure occurs only when all n machines are in the failed condition at the same time. A penalty cost is assessed for system failure, this cost being proportional to the system down-time. Case 2—When n machines are operated as in Case 1, except that any machines which fail are not returned to operation until the beginning of the next operating period. Penalty cost for system failure is assessed in the same way as in Case 1. Case 3—Where n machines are operated as in Case 2, but where the penalty cost for system failure is a fixed amount and is independent of the resulting down-time.

436
An Approach to Airborne Digital Computer Equipment Construction, by P. E. Boron and E. N. King (Hughes Aircraft Co.); IRE Trans. on Production Techniques, vol. PT-4, pp. 18–21; June, 1959.

A method of building airborne digital equipment which makes use of the modularized etched-wiring plug-in philosophy and which utilizes an all-etched-wiring harness to accomplish the entire complex of connections between plug-in units is discussed. Of a possible 364 external connections, 183 are actually brought to a possible 1716 connector contacts. These contacts and their associated printed wiring tie together 32 flip-flop modules and 17 diode-gating etched-pattern matrix arrays without the use of a single piece of conventional wiring. Points of emphasis are miniaturization, reliability, small weight, accessibility, and manufacturability of the equipment.

437
A Digital Computer System for Terminal-Area Air Traffic Control, by E. L. Braun (Genesys Corp.) and A. S. Gianoplus (Litton Industries); IRE Trans. on Space Electronics and Telemetry, vol. SET-5, pp. 66–72; June, 1959.

The terminal-area air traffic control (ATC) operation is defined, and a classification of its problem areas which demonstrates the need for both general-purpose computation and special-purpose data processing is provided. The characteristics of the digital-computing equipment for the functions of tracking, scheduling, and guidance are described. The overall capabilities of the system are presented, including a description of the facilities for entry, sensing, communication, and display of pertinent data.

B-2: SYSTEMS—DESCRIPTIONS

438
The Univac Solid-State 80 Computer; *Univac Rev.*, vol. 2, no. 2, pp. 4–5; Summer, 1959.

The Univac solid-state 80 computer is briefly described. With its large 50,000-digit drum memory and 17-microsecond word time, the machine is ideal for table look-up operations. Another feature is the biquinary code which enables the conventional 80-column card to be "stretched" to carry considerably more information than normal.

439
PILOT—A New Multiple Computer System, by A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger (Natl. Bur. of Standards); *J. Assoc. Comp. Mach.*, vol. 6, pp. 313–335; July, 1959.

The PILOT data processor, a new high-speed multiple computer system, is described. The three interconnected computers contribute to an extremely fast, versatile and flexible system that can accept input and produce output in any convenient form. A first general-purpose machine handles the arithmetic and logical operations, a second computer is responsible for bookkeeping and "red-tape," while the third monitors all input-output.

440
Processing Data in Bits and Pieces, by F. P. Brooks, Jr. G. A. Blaauw, and W. Buchholz (IBM Corp.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 118–124; June, 1959.

A data-handling unit which permits binary or decimal arithmetic to be performed on data fields of any length from one to sixty-four bits is described. Within the field, character structure can be further specified: these processing entities, called bytes, may be from one to eight bits long. Fields may be stored with or without algebraic sign. On all operations, the relative offset or shift between the operand from memory and that from the accumulator can be specified. Besides the arithmetic operations, three new logical instructions allow any of the sixteen logic connectives of two variables to operate upon each pair of bits in the memory and accumular operands. The variable field length, variable byte-size features extend the use of connective operations to a surprisingly wide variety of logical, housekeeping, and editing tasks. These arithmetic and connective instructions are general and powerful programming tools which greatly simplify complex manipulations. Programming of typical tasks, with both the new instructions and with the instruction set of a conventionally-organized computer, has shown that the new set requires substantially fewer instructions to be written, stored, and executed. Furthermore, the new instruction set has considerably fewer distinct operations than the more conventional set. This is possible because the general-purpose instructions of the new set replace many ad hoc instructions which deal with pieces of instructions or data words, or which perform shifting, packing, or editing functions. The initial application of the variable field length data-processing unit is in the IBM STRETCH computer.

441
Air Traffic Control Computer, by A. G. Van Alstyne and M. H. Notham (Gilfillan Brothers, Inc.); 1959, IRE National Convention Record, pt. 5, pp. 26–34.

A special-purpose digital machine intended for use in an en-route air traffic control application is described. The primary function of the computer is to clear flight plans by checking for conflict with previously cleared flight plans and to reroute as necessary to avoid conflict. A secondary function is that of tracking and flight following, enabling aircraft progress to be monitored for conformance to plan; in cases of nonconformance the affected flights are automatically rescheduled. A third function is the continuous check of all flights for possible predicted conflict and issuance of control orders to resolve conflict. The evolution of a consistent and practical control philosophy is discussed, and the various functions which must be performed to implement the chosen approach are outlined. Each of these functions is then discussed in relation to its significance for computer parameters and programming configurations. The computer configuration required by these functions is considered and the special characteristics required by the problem are emphasized. The computer capabilities and those of available equipments are compared.

442
The Automatic Position Survey Analyzer and Computer, by F. J. Alterman (General Mills, Inc.); 1959 IRE National Convention Record, pt. 4, pp. 231–241.

The Automatic Position Survey Equipment which is used to conduct first-order astronomic surveys of the earth's surface and the APSAC digital computer which is part of this equipment are described. The basic component of the computer, the Logic Unit Board, which is a transistorized digital component from which other computers and data handling systems can be constructed simply and at low cost, is also described.

443
An Analog Computer for Finding an Optimum Route Through a Communication Network, by H. Rapaport and P. Abramson (RCA Surface Communications Systems); IRE Trans. on Communications Systems, vol. CS-7, pp. 37–42; May, 1959.

An analog computer capable of solving a variety of communication network problems, in particular the problem of finding an optimum route through an arbitrary network, is described. For example, in routing a call through a communications network, it may be desirable to determine that path (or paths) containing the smallest number of switching centers; or again, if, in some predetermined sense, weighting factors have been assigned to each link in the network, it is then possible to determine that path over which the summation of the weights of the links is a minimum. A 16-node multiply-connected prototype has been designed in which "time" is used as the analog of link weights. The utilization of this prototype to find minimum paths and the relative merit of alternate paths are described. The prototype also has the capacity of simulating network vulnerability (link or node inhibition of destruction).

444
A Real Time Data Assimilator, by H. W. Gschwind (Holloman Air Force Base); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 33–36; July, 1959.

A real-time data assimilation system in which input is read directly into ancillary storage registers, by-passing conventional buffers, is described. These special registers, called loading platforms, like normal memory registers may be referred to by arithmetic and logic instructions and differ only in that interlocks prevent their being written on. Output is treated analogously. The system provides for real-time manipulation of data from many sources.

B-3: SYSTEMS—APPLICATIONS

445
A System for Editing and Computer Entry of Flight Test Data, by S. F. Higgins (Consolidated Electrodynamics Corp.); 1959 IRE National Convention Record, pt. 5, pp. 166–175.

A system of data editing with provisions for computer entry of flight test data as required by an integrated digital data system is described. System concepts which must be dealt with in solving this type of problem are described. The computer station is provided with editing control facilities that permit selection of the desired prime and commutated channels which are essential for data reduction. The editing facilities provide for the most economic use of computer and manpower effort and are so designed that they permit convenient access to all instrumented channels. Peripheral equipment is also described as an aid in the editing process for examining the new data in terms of analog, quick look, and permanent record equipment.

B-4: SYSTEMS—TESTING

446
Experiments on the Relation of the Operator to the Control Loop of an Airborne Digital Computer, by C. A. Bennett (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 275–281; July, 1959.

Laboratory experiments performed over a period of three years to provide design information for digital computer systems for error correction in aircraft navigation are discussed. In a simulated digital control loop, the operator observed crosshair error and fed control signals to the computer. The studies showed relationships between recovery time and solution rate, transmission delays, hand-control sensitivity, sampling rate, and scanning rate.

C-2: AUTOMATA—ARTIFICIAL

447
A Learning Machine: Part II, by R. M. Friedberg, B. Dunham, and J. H. North (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 282–287; July, 1959.

An effort is made to improve the performance of the learning machine described in Part 1 and the over-all effect of various changes is considered. Comparative runs by machines without the scoring mechanism indicate that the grading of individual instructions can aid in the learning process. A related study is made in which automatic debugging of programs is taken as a special case of machine search. The ability to partition problems and to deal with parts in order of difficulty proves helpful.

448
Some Studies in Machine Learning, Using the Game of Checkers, by A. L. Samuel (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 211–229; July, 1959.

A detailed investigation of two machine-learning procedures using the game of checkers is discussed. Enough work has been done to verify the fact that a computer can be programmed so that it will learn to play a better game of checkers than can be played by the person who wrote the program. Furthermore, it can learn to do this in a remarkably short period of time (8 or 10 hours of machine-playing time) when given only the rules of the game, a sense of direction, and a redundant and incomplete list of parameters which are thought to have something to do with the game, but whose correct signs and relative weights are unknown and unspecified. The principles of machine learning verified by these experiments are, of course, applicable to many other situations.

449
A General Problem-Solving Program for a Computer, by A. Newell and J. C. Shaw (The Rand Corp.) and H. A. Simon (Carnegie Inst. Tech.); *Computers and Automation*, vol. 8, pp. 10–17; July, 1959.

A general problem-solving technique based on the use of heuristic principles is described. Among the principles are functional or means-end analysis, planning, and subgoal reduction. Illustrative examples of simple problem solutions in symbolic logic, trigonometry, and chess are presented. Programs to solve problems in particular fields may be prepared from the general principles.

450
Restoring Organs in Redundant Automata, by O. Lowenschuss (Lewyt Manufacturing Co.); *Information and Control*, vol. 2, pp. 113–136; June, 1959.

Redundant automata, as described by von Neumann, use "restoring organs" in order to remove the effect of malfunctions. It is shown that the class of possible restoring organs is wider than that discussed by von Neumann. If "triplication" is used, a class of majority elements for the multivalued case provides restoring action in approximately the same amount as von Neumann's two-valued majority organs. If "multiplexing" is used, possible restoring organs can be classified in terms of their "length." The length-1 restoring organs are majority elements; the length-2 restoring organs are derived from the majority organ concept, etc. This approach makes it possible to write truth-tables for restoring organs, and to synthesize them by means of two-valued or multivalued devices.

D-1: PROGRAMS—AUTOMATIC PROGRAMMING, DIGITAL COMPUTERS

451
Automatic Programming Systems, *Commun. Assoc. Comp. Mach.*, vol. 2, p. 16; May, 1959.

A table of the more widely known computing machines, with the names of the automatic programming systems associated with each, is given. The table includes the IBM 700 series, IBM 650, Univacs I and II and 1103, Datatron 201–205, Whirlwind and Ferranti's Mercury and Pegasus machines.

452
Handling Identifiers as Internal Symbols in Language Processors, by A. F. Williams (IBM Corp.); *Commun. Assoc. Mach.*, vol. 2, pp. 21–24; June, 1959.

A method whereby programming tags or identifiers need not be confined to the length of the machine word is outlined. An algorithm assigns numeric values to the external tags, and then maps these values onto a set of integers of limited range which are the internal tags. The processor, or compiler, converts these internal tags into memory locations within the machine. Much redundancy in information content is avoided, and the programmer is free to choose tags to suit his mnemonic convenience.

453
On GAT and the Construction of Translators, by B. Arden and R. Graham (University of Michigan); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 24–26; July, 1959.

The salient features of the Generalized Algebraic Translator (GAT) developed at the University of Michigan are described. The system was developed for an IBM 650 machine with index registers.

454
Thaumaturgy: A Simplified Method of Coding for Ordvac, by M. J. Romanelli (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 32, p. 93(A); July 17, 1959. PB 139 928 (Order from LC, Mi $4.50, Ph $13.80).[1]

A simplified method of coding which enables one to use the services of Ordvac, a high-speed computing machine, is discussed. Emphasis has been placed on simplicity so that no previous experience in coding for high-speed computing machines is required. Illustrative examples are included.

D-2: PROGRAMS—APPLICATIONS, DIGITAL COMPUTERS

455
The Application of a Computer to Bank Accounting, by B. W. Taunton (First National Bank of Boston); *Computers and Automation*, vol. 8, pp. 18–25; July, 1959.

Data processing problems associated with banking are discussed and the development of a system to handle deposit accounting and corporate trust operations is outlined. Careful analysis and definition of objectives and criteria for the feasibility and selection of equipment are stressed.

456
Application of the NCR 304 Data Processor to the Synthesis of a Digital Computer Building Block, by G. H. Goldstick and M. Kawahara (National Cash Register Co.); 1959 IRE National Convention Record, pt. 4, pp. 204–217.

The use of the NCR 304 Data Processor to synthesize a transistorized digital computer building block is discussed. The building block consists of a tape-wound core /transistor regenerative amplifier which is the principal component in SCAN, a solid-state account number checking device. Since the cost of the accounting machine is a sensitive function of the cost of the amplifier and since an extensive production run for the machine was contemplated, optimization of the amplifier was thought necessary.

457
A Comparison of Methods for Generating Normal Deviates on Digital Computers, by M. E. Muller (Princeton University and IBM Corp.); *J. Assoc. Comp. Mach.*, vol. 6, pp. 376–383; July, 1959.

Various methods, including two new ones, for generating pseudo random normal deviates within a computer are compared. All assume the existence of a satisfactory source of random numbers. The two new methods, one a direct and the other an inverse approach, yield gains in accuracy and speed. A table of timing, precision, and memory space in an IBM 704 computer relating to each method is presented.

458
Determination of Schmerling Coefficients by Digital Computer Techniques Including Tabulated Values for Magnetic Dip Angles Between 0° and 80°, by C. A. Ventrice and E. R. Schmerling (Pennsylvania State University); *U. S. Govt. Res. Repts.*, vol. 32, pp. 34–35(A); July 17, 1959. PB 135 878 (Order from LC, Mi $3.30, Ph $7.80).[1]

A digital computer program for the computation of coefficients by means of which HF records may readily be reduced to *N-h* profiles without further computational aids is developed. Full account is taken of the earth's magnetic field, and no special layer-shapes are assumed. Tables of these coefficients which are valid over most of the earth except where the magnetic dip exceeds 80° are computed. The accuracy of the coefficients and their sensitivity to the magnetic field parameters are discussed. Conclusions are drawn, from actual examples, concerning the use of the tables, and the over-all accuracy which may be expected in their use.

459
Automatic Lens Design by the Least Squares Method, by J. Meiron (Ministry of Defense, Israel); *J. Opt. Soc. Am.*, vol. 49, pp. 293–298; March, 1959.

Lens design by the least squares method on the Weizmann Institute of Science electronic digital computer is discussed. The least squares method permits the simultaneous variation of a large number of design parameters. The minimization process is iterated until a satisfactory solution is obtained. Two programs are described, for the correction of third-order aberrations and of residual aberrations, respectively. The time required to complete one iteration is 0.5 second per surface per parameter for the first program, the corresponding time for the final correction being 3.5 seconds. Examples of actual applications of the method for the correction of a Cooke triplet and of a Tessar system are presented.

460
Lens Designing by Electronic Digital Computer: I, by C. G. Wynne [Wray (Optical Works) Ltd.]; *Proc. Phys. Soc.*, vol. 73, pp. 777–787; May, 1959.

The problem of automatic lens designing by an electronic digital computer is considered in the light of existing aberration theory. Methods previously suggested are discussed, and a new iterative method of linear approximation is described.

461
A Monte Carlo Code for Gamma Ray Transmission Through Laminated Slab Shields, by R. A. Liedtke and H. A. Steinberg (Tech. Res. Group); *U. S. Govt. Res. Repts.*, vol. 31, pp. 360–361 (A); May 15, 1959. PB 151 605 (Order from OTS, $2.75).[1]

An IBM 704 Monte Carlo code for computing the transmission of monoenergetic and monodirectional gamma rays by a multilayered slab geometry shield is described. The main output data are the total energy current and flux. The associated energy spectra of each accompanied by their standard deviations are also obtained but at lesser accuracy. Extensive use is made of variance reduction techniques, including use of calculated first collision points, a modified form of the exponential transformation, and a statistical estimation of the transmission after each collision. Importance sampling is used for choosing the recoil energy and the change in azimuthal angle following collision. Results are quoted for Compton scattering medium and for a selected group of one, two, and three slab lead-water shields. Comparisons are made with infinite medium results corrected in a plausible manner for edge effects. They are interpreted as permitting the use of an empirical formula due to M. Kalow for two-slab lead-water shields for a large number of situations of interest. The energy spectra are also discussed.

462
Digital Computer Determination of Low Frequency Polarization, by A. J. Ferraro (Pennsylvania State University); *U. S. Govt. Res. Repts.*, vol. 32, p. 131(A); July 17, 1959. PB 140 144 (Order from LC, Mi $3.30, Ph $7.80).[1]

The results of a rapid method for determining the polarization of low frequency echoes which include the effects of collisions and the earth's magnetic field are compared with those of the multislab approximation. It is shown that the method yields satisfactory results. For two electron density profiles (one near critical coupling and one far removed) the Rydbeck coupling region was subdivided into slabs of uniform media; by matching the fields between adjacent slabs, $N-1$ simultaneous equations (for N slabs) were obtained.

463
A Technique for Computing Critical Rotational Speeds of Flexible Shafts on an Automatic Computer, by B. L. Schwartz and H. A. Cress (Battelle Memorial Institute); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 27–31; June, 1959.

The basic differential equation

$$\frac{d^2}{dx^2}\left[EI\frac{d^2y}{dx^2}\right] = \mu\omega^2 y$$

describing the critical rotational speeds of a flexible shaft is derived from beam theory. The differential equation is transformed into a set of recursion relations for computer solution by breaking the shaft into n sections of length $(\Delta x)_n$.

464
A Gas Film Lubrication Study, by W. A. Gross, W. A. Michael, R. K. Brunner, J. M. Harker, K. E. Haughton, and A. G. Osterlund (IBM Corp.); *IBM J. Res. & Dev.*, vol. 3, pp. 237–274; July, 1959.

The Reynolds differential equation describing flow in a compressible lubricating film is developed, and a finite-difference technique for obtaining approximate numerical solutions to the equation is presented. A digital computer program is described and discretization errors and stability of the difference equations are discussed. Pressure, load, velocity, and geometry characteristics are presented for many compressible slider bearing films based upon the computer solutions. Experimental verification of the computer solutions is discussed and experimental techniques are described.

465
The Anisotropic Structure Refinement of 4-Methyl-1, 2-Dithia-4-Cyclopentene-3-Thione on an IBM Type 650 Computer, by G. A. Jeffrey and R. Shiono (University of Pittsburgh); *Acta Crystall.*, vol. 12, pp. 447–454; June, 1959.

An anisotropic refinement of the structure of 4-methyl-1,2-dithia-4-cyclopentene-3-thione, $S_2C_4H_4$, carried out on an IBM 650 computer using the differential Fourier synthesis technique, is discussed. Although the shifts in atomic coordinates were small, the thermal anisotropy was appreciable and the convergence of the refinement was slow in that six cycles of refinement were required. The difference in molecular dimensions as compared with the results from isotropic analysis reported previously were less than 0.54Å, but the standard deviations, as calculated by Cruickshank's method, were halved with a corresponding reduction in the agreement index.

466
Solution of Thermochemical Propellant Calculations on High-Speed Digital Computer, by A. J. Donegan and M. Farber (California Inst. Tech.); *U. S. Govt. Res. Repts.*, vol. 31, p. 332(A); May 15, 1959. PB 139 031 (Order from LC, Mi $2.70, Ph $4.80).[1]

The use of a high-speed digital computer to carry out performance calculations on rocket fuels is discussed. Mathematically

the problem resolves to the simultaneous solution of a group of nonlinear algebraic equations which yield gas composition, flame temperature, average molecular weight, exhaust velocities, and other performance parameters. A three-cycle iterative scheme has been developed for the simultaneous solution for the various components involved in chemical combustion phenomena. Following the iteration, a straightforward computation obtains the performance parameters. With the present floating-decimal programming, the digital computer provides a complete solution for propellant performance calculations in an average time interval of approximately 30 minutes. The computing time previously required for the solution of these problems by desk calculation was measured in terms of days. Introduction of fixed-decimal methods would diminish the average time required per solution to approximately five minutes.

467
From Flight Variables to Heart Beats, by C. G. Peckham (University of Dayton, Ohio); *Univac Rev.*, vol. 2, pp. 28–29; Summer, 1959.

Data processing activities in the fields of aviation and applied medicine being carried out at the University of Dayton are described.

468
A Program to Score Rating Scales on the IBM Type 650, by C. E. Wright and P. Horst (University of Washington); *U. S. Govt. Res. Repts.*, vol. 32, p. 93(A); July 17, 1959. PB 140 179 (Order from LC, Mi $1.80, Ph $1.80).[1]

A program which scores rating scales of up to 483 items, producing up to 21 trait scores where each trait is represented by a subset of not more than 23 items, is discussed. All item scores must be positive numbers of one, two, or three digits, and all trait scores are punched as three digit numbers with the location of the decimal point determined from information provided on a parameter card. The input card form is that of the basic statistics program. The output card form is identical with the input card form so that the trait scores obtained can be further analyzed immediately by employing the basic statistics or correlation matrix programs.

469
Programming a Combinatorial Puzzle, by D. S. Scott (Princeton University); *U. S. Govt. Res. Repts.*, vol. 32, p. 93(A); July 17, 1959. PB 139 963 (Order from LC, Mi $2.70, Ph $4.80).[1]

The programming of a variant of the geometrical placement puzzle called "pentominos" for the von Neumann computer, in order to study the difficulties of communicating well-posed problems to digital computers, is discussed. The logical difficulties which were encountered and solved are covered. Solutions to the puzzle are given.

470
Automatic Programming Answers a Need, by R. S. Bingham, Jr. (The Carborundum Co.); *Univac Rev.*, vol. 2, pp. 6–11; Summer, 1959.

The use of the Univac Math-Matic Automatic Programming system for quality control problems is described. As most of the applications are "one-shot," the reduction in coding and debugging time resulting from the system is particularly important.

471
Blueprint for Automatic Inventory Control, by R. S. Jones (Boston Motor Parts Co.); *Univac Rev.*, vol. 2, pp. 22–27; Summer, 1959.

An automatic inventory control system operated by a large wholesaler is described. Input is from punched cards to a small special-purpose computer which handles customer billing, discounts, commissions and automatic reordering when inventory falls below preset quantities. Improved customer service and integrated processing of paper work at reduced cost result from the introduction of the system.

472
Electronic Digital Machines for High-Speed Information Searching, by P. R. Bagley (M.I.T.); *U. S. Govt. Res. Repts.*, vol. 31, p. 345(A); May 15, 1959. PB 135 440 (Order from LC, Mi $7.20, Ph $22.80).[1]

Methods and machines designed to make possible the high-speed location of related items in a large body of suitably indexed information are examined. It is shown that without major modifications an electronic digital computer designed for general mathematical work is inherently unsuited to the information searching process. It is possible, however, to construct an electronic machine from standard digital computer components (flip-flops, gates, etc.) which would be capable of scanning the index to nearly 5 million documents per hour (at 900 binary digits per document) and of preparing a list of the serial numbers of the selected documents. Metal magnetic tape seems to be the most suitable storage medium for the index.

473
On Computer Transcription of Manual Morse, by C. R. Blair (Dept. of Defense); *J. Assoc. Comp. Mach.*, vol. 6, pp. 429–442; July, 1959.

The problems of transcription of manual Morse code resulting from the nonregularity of timing and differences between operators are analyzed and a statistical solution is described. The machine continuously monitors a "goodness of separation" statistic between the key-down dots and dashes and key-up intra- and intercharacter signals, and adjusts its threshold points accordingly. A comparison of the computer's transcription performance with that of human rivals indicates that it does at least as well.

D-3: PROGRAMS—TECHNIQUES, DIGITAL COMPUTERS

474
Programming for a Machine with an Extended Address Calculational Mechanism, by H. Schecher (Technische Hochschule, Munich, Ger.), translated by J. W. Carr, III (University of Michigan); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 32–38; June, 1959.

A method to make all the registers of a high-speed memory available as index registers is presented. The increase in technical expense would be confined to a small arithmetic register that has only to perform addition and a substitution register in addition to the coincidence register, together with the necessary interconnections. Great versatility in instruction modification and cascading of subroutines and loops are desirable by-products of the method.

475
Representation of Switching Circuits by Binary-Decision Programs, by C. Y. Lee (Bell Telephone Labs., Inc.); *Bell Sys. Tech. J.*, vol. 38, pp. 985–999; July, 1959.

The relationship between switching circuits and binary-decision programs is shown and a set of simple rules by which one can transform binary-decision programs to switching circuits is given. It is shown that, in regard to the computation of switching functions, binary-decision programming representation is superior to the usual Boolean representation.

476
The Storage Problem, by W. S. Cooper (M.I.T.); *Mech. Translation*, vol. 5, pp. 74–83; November, 1958.

Methods for making optimum use of the limited capacity of high-speed memories in handling the bulky linguistic reference data necessary for machine translation are reviewed. A procedure for compressing a dictionary and yet retaining its full usefulness is described. The method introduces no chance of look-up error, provided the item to be looked up is in the dictionary.

477
A High-Speed Sorting Procedure, by D. L. Shell (General Electric Co.); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 30–32; July, 1959.

A sorting procedure combining some of the properties of merging and sifting that makes optimum use of a large, high-speed memory is described. The method can fit twice as many items at one time in memory as a merge-sort with very little sacrifice in speed.

478
The Cumulative File Problem, by W. H. Minor (Warner Robbins Air Materiel Area); *Univac Rev.*, vol. 2, pp. 18–21; Summer, 1959.

The extraction of a cumulative file of active items from the master file is proposed as a means of reducing updating time for large files. A mathematical model of file activity, depending on size of master file, proportion of active items in it, and average number of daily transactions, from which the composition and length of the cumulative file may be predicted, is presented.

479
Unnormalized Floating Point Arithmetic, by R. L. Ashenhurst and N. Metropolis (Uni-

versity of Chicago); *J. Assoc. Comp. Mach.*, vol. 6, pp. 415–428; July, 1959.

Algorithms for floating point arithmetic in which the mantissa is not subject to the usual normalization convention are described. Advantages are that results are given in a form indicative of their precision and that ambiguities associated with a zero mantissa are resolved. An analysis of one-stage error propagation for each arithmetic operation is developed, and a statistical model for long-range error propagation is set forth. Investigations indicate that implementation is not as difficult as might appear and that operation times are shorter.

480

Binary Conversion, with Fixed Decimal Precision, of a Decimal Fraction, by D. Taranto (IBM Corp.); *Commun. Assoc. Comp. Mach.*, vol. 2, p. 27; July, 1959.

An algorithm to find a binary approximation to a given decimal with a given decimal precision is presented. The algorithm is then stated as an International Algebraic Language (IAL) procedure.

481

An Orbit Program for Engineering Use, by B. H. Bloom and H. R. Smith (Radio Corp. of America); 1959 IRE National Convention Record, pt. 5, pp. 240–250.

A philosophy of programming digital computers for engineering applications is presented. The concept of "minimum answer time" serves as a basis for this philosophy. Several programming techniques, which are implementations of this philosophy, are discussed. A program for computing ballistic trajectories and orbits is described as an application of these abstract programming concepts to a practical engineering problem.

D-5: PROGRAMS—APPLICATION, ANALOG COMPUTERS

482

Generalized Integration on the Analog Computer, by G. A. Bekey (Space Technology Labs., Inc.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 210–217; June, 1959.

The usual methods of overcoming the inability of an electronic analog computer to perform an integration with respect to a dependent variable directly are reviewed, the results of an attempt to use Padé time-delay units in generalized integration are described, and the development of a new analog integrator based on a simple numerical integration formula is presented. The integrator can be instrumented using standard analog computer components. The performance of the device is illustrated with several examples.

483

Linear System Approximation by Differential Analyzer Simulation of Orthonormal Approximation Functions, by E. G. Gilbert (University of Michigan); IRE Trans. on Electronic Computers, vol. EC-8, pp. 204–209; June, 1959.

An analytic procedure for minimum integral-square-error approximation of prescribed linear systems in which a group of N linear approximating systems with orthonormal impulse responses $\phi_n(t)$ are realized by operational amplifier circuits is discussed. When $h(-t)$ forces the systems [$h(t)$ is the impulse response of the prescribed system], it is found that their outputs at $t=0$ are a_n, the coefficients in

$$h^*(t) = \sum_{n=1}^{N} a_n \phi_n(t),$$

the approximate impulse response. The following points relative to the approximation procedure are developed: constrained and weighted integral-square-error approximations, derivation and realization of orthonormal functions, physical realization of $h^*(t)$, evaluation of error $h(t)-h^*(t)$, and analysis of computer errors. Several approximation examples are given.

484

The Use of a Repetitive Differential Analyzer for Finding Roots of Polynomial Equations, by P. Madich, J. Petrich, and N. Parezanovich (Inst. of Nuclear Sciences, Belgrade); IRE Trans. on Electronic Computers, vol. EC-8, pp. 182–185; June, 1959.

A procedure for obtaining real and complex roots of algebraic equations with real or complex coefficients by the use of a repetitive differential analyzer is described. The procedure requires only operational amplifiers and ganged linear potentiometers. Differential analyzers are very suitable for solving algebraic equations since they permit visual checking of the procedure and make it possible to investigate how the roots of the polynominal are affected by variation of its coefficients. The procedure is not iterative.

485

Optimization by Random Search on the Analog Computer, by J. K. Munson (E. I. DuPont de Nemours and Co.) and A. I. Rubin (Electronic Associates, Inc.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 200–203; June, 1959.

One method of searching a system for optimum operating conditions is to evaluate system performance for many randomly-chosen combinations of the independent parameters. The use of standard electronic analog computer equipment to accomplish such a search of a mathematical model quickly and economically is discussed. Gaussian noise sources generate values of the independent parameters and sample-hold circuits hold those values which give the best value of the optimization criterion. An application of the method to a production allocation problem is described.

486

A Perturbation Technique for Analog Computers, by L. Bush and P. Orlando (Cornell Aeronautical Lab., Inc.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 218–221; June, 1959.

A study of the motion of a fin-stabilized rocket, undertaken to determine the effect of perturbing forces on the trajectory, is discussed. The mechanization of a complete problem for an analog computer to include small disturbing forces would result in trajectories which are essentially indistinguishable from the "nominal" or "unperturbed" case because of analog computer accuracy limitations. Instead, the equations of motion for the "nominal" case and the "perturbed" case, derived by first-order ballistic perturbation theory, were solved simultaneously with the nominal solution providing inputs to the perturbed solution. The analog computer solution provided both the nominal trajectory and the perturbations from this trajectory. To illustrate the method, the technique is applied to the two-dimensional motion of a rocket in the vertical plane and includes perturbations due to uncertainties in winds, atmospheric density, thrust malalignments, and stability margin.

487

Pulsed Analog Computer for Simulation of Aircraft, by A. W. Herzog (U. S. Naval Training Device Center); Proc. IRE, vol. 47, pp. 847–851; May, 1959.

The logical design of a pulsed analog-digital computer which can be used to solve the system of nonlinear differential equations normally encountered in the simulation of aircraft is described. The design calls for a magnetic drum to perform the functions of storing the program and the aerodynamic data required in the computation. Time-shared analog computing elements encompassing the normal arithmetic operations of addition, subtraction, multiplication, and division are used. They are connected to a common bus through gating circuits. In addition, electronic integrators (one for each integration required) and analog-storage elements are provided. Utilizing these elements sequentially, it is possible to complete a computation cycle in each revolution of the drum. Function generation is accomplished by means of specialized circuitry which determines the position of the four surrounding break points of a given value of a function of two or more variables. The discrete values of the function at the break points are selected from digital drum storage for an interpolation procedure. A type of "floating point" system is included to scale automatically all voltages to fall within optimum levels for the operating elements. The computer appears to offer the advantages of flexibility, compactness, ease of programming, and economy commensurate with the limited accuracies required in flight-training simulation.

488

Radar Systems Simulation Techniques, by J. Lambert and A. Heidrich (General Electric Co.); 1959 IRE National Convention Record, pt. 4, pp. 190–203.

Analog computer circuits which can be combined to simulate complete radar systems are presented. Computer circuits which can be used to simulate radar components such as RF filters, mixers, IF amplifiers, phase and amplitude detectors, video amplifiers, delay lines, limiters, klystrons , magnetrons, etc., are developed. Scale factors, stability, and methods of simulator checking are discussed. The complete simulation of a

phase-locked radar guidance system is used to illustrate the application of the computer circuits.

489
Calculation of Explosion Products at Equilibrium by Analog Computer, by A. G. Edwards and A. I. Rubin (Picatinny Arsenal); *U. S. Govt. Res. Repts.*, vol. 31, pp. 440(A); June 12, 1959. PB 137 578 (Order from LC, Mi $2.70, Ph $4.80).[1]

The use of the analog computer in the solution of the theoretical equations that are used in calculating the explosion or isochoric adiabatic flame temperature of explosives is described. The computer is used to solve a set of nonlinear simultaneous equations which are the result of a series of algebraic simplifications of the equilibrium equations. The solutions of these equations are used to calculate the combustion products and these values are in turn used to calculate the explosion temperature. The technique by which these particular nonlinear simultaneous equations are handled on the computer can also be applied to the solution of other equations of this general type.

490
Distributed Parameter Vibration with Structural Damping and Noise Excitation, by R. V. Powell (California Inst. Tech.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 197–200; June, 1959.

A method for the determination on an electronic analog computer of the vibration amplitude responses of a distributed system with structural damping to a random-noise excitation is discussed. Such a situation exists when a missile structure is accelerated by a jet propulsion system. There is general agreement among the investigators in the literature that structural damping is both frequency independent and amplitude dependent. Simulation of the structure by a method of normal modes permits the introduction of a discrete equivalent viscous-damping coefficient for each mode frequency, thus effecting the frequency-in-dependent characteristic of structural damping.

491
Analog Computer Measurements on Saturation Currents, Admittances and Transfer Efficiencies of Semiconductor Junction Diodes and Transistors, by A. H. Frei and M. J. O. Strutt (Swiss Federal Inst. of Tech.); Proc. IRE, vol. 47, pp. 1245–1252; July, 1959.

The use of an analog computer to determine saturation currents of junction diodes and ac admittances and transfer efficiencies of transistors is discussed. The computer takes into consideration diffusion, and bulk and surface recombination in three-dimensional structures with rotational symmetry around an axis. Good agreement was found between the measured and computer values of saturation currents and admittances of three batches of diodes. Some unexpected features of the computer curves are that the ratios of saturation currents obtained from the analog computer and from one-dimensional solutions exceed unity and may be as high as 2. Similar figures hold for ac admittances. Some choices of transistor dimensions, leading to high transfer efficiencies, are suggested by the computer curves.

E-1: MATHEMATICS—LOGIC—THEORETICAL MATHEMATICS

492
Analysis of Binary Time Series in Periodic Functions, by P. J. Van Heerden (General Electric Res. Lab.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 228–229 (L); June, 1959.

A Fourier-like analysis for a binary time series (defined only for $t=0, 1, 2$, etc., and with values either 0 or 1) is discussed. The binary analysis is similar to the Fourier series since the functions in which a binary time series can be analyzed are periodic. It differs from the Fourier analysis since the periods are n, $1/2n$, $1/4n$, $1/8n$, etc. (down to period 1), where n is the total length of the series, and since the binary analysis is possible only for a length $n=2^p$. In the binary case, the functions are not mutually orthogonal.

E-2: MATHEMATICS—LOGIC—SYMBOLIC LOGIC, BOOLEAN ALGEBRA, NUMBER SYSTEMS

493
A New Operation for Analyzing Series-Parallel Networks, by K. E. Erickson (The Johns Hopkins University); IRE Trans. on Circuit Theory, vol. CT-6, pp. 124–126; March, 1959.

The operation $*$, defined as $A*B=AB/(A+B)$, is introduced. The symbol $*$ has algebraic properties which simplify the formal solution of many series-parallel network problems. If the operation $*$ were included as a subroutine in a digital computer, it could simplify the programming of certain network calculations.

494
Canonical Forms for Information-Lossless Finite-State Logical Machines, by D. A. Huffman (M.I.T.); Special Supplement to IRE Trans. on Circuit Theory, and on Information Theory, vol. CT-6 and vol. IT-5, pp. 41–59; May, 1959.

An important class of finite-state machines transforms input sequences of digits into output sequences in a way such that, after an experiment of any finite length on the machine, its input sequence may be deduced from a knowledge of the corresponding output sequence, its initial and final states, and the set of specifications for the transformations by which the machine produces output sequences from input sequences. These machines are called "information-lossless." Canonical circuit forms into which any information-lossless machines may be synthesized are shown. The existence of inverses for these circuits is investigated, and circuits for their realization are derived.

495
Mathematical Models for Sequential Machines, by S. Seshu (University of Toronto); 1959 IRE National Convention Record, pt. 2, pp. 4–16.

A unified introduction to the various mathematical models which have been developed for sequential machines in recent years is presented. The models discussed are due to Moore, Mealy, Huffman, and Muller. The Moore state diagram is taken as the basic model in terms of which the others are introduced. The applications of these models to machine design is briefly considered. Although complete synthesis procedures are not included, a bibliography of papers on the subject is presented.

496
Transition Matrices of Sequential Machines, by S. Seshu (University of Toronto), R. E. Miller (IBM Corp.), and G. Metze (University of Illinois); IRE Trans. on Circuit Theory, vol. CT-6, pp. 5–12; March, 1959.

A matrix technique for the analysis of state diagrams of synchronous sequential machines is introduced. The matrices are closely related to the relation matrices of the calculus of relations and provide a formal tool for discussing state diagrams. It is shown that several of the well-known theorems on state diagrams are consequences of properties of transition matrices, which remain invariant under matrix multiplication. A reduction procedure for state diagrams, based on transition matrices, which is similar to Moore's technique, is given. A method of extending the results to asynchronous machines is also included.

497
The Theory of Switching Nets, by M. Yoeli (Israel Inst. Tech.); Special Supplement to IRE Trans. on Circuit Theory and on Information Theory, vol. CT-6 and vol. IT-5, pp. 152–157; May, 1959.

A strictly mathematical unified theory of combination switching networks is developed with the aid of linear graph theory and lattice algebra. The theory is based on the concept of a lattice-weighted, directed linear graph, termed a switching net. The advantages of using lattice algebra, rather than Boolean algebra, are emphasized. A calculus of lattice matrices is outlined and then applied to the study of switching nets. A suitable formulation of Ashenhurst's uniqueness theorem and a modified version of its proof are given. Switching net theory is extended to multiterminal and reiterative nets, generalizing results due to M. L. Tsetlin and A. Sh. Blokh.

498
Hazards and Delays in Asynchronous Sequential Switching Circuits, by S. H. Unger (Bell Telephone Labs., Inc.); IRE Trans. on Circuit Theory, vol. CT-6, pp. 12–25; March, 1959.

Asynchronous, sequential switching circuits in which the variables are represented by voltage levels, not by pulses, are discussed. The effects of arbitrarily located stray delays in such circuits are analyzed, and it is shown that, for a certain class of functions, proper operation can be assured regardless of the presence of stray delays and without the introduction of delay elements by the designer. All other functions require at least one delay element in their circuit realizations to insure against hazards. In the latter case, it is shown that a single delay element is always sufficient. The price that must be paid for minimizing the number of delay elements is that of greater circuit complexity.

499
Linear Modular Sequential Circuits, by B. Friedland (Columbia University); IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 61–68; March, 1959.

Sequential circuits comprising 1) modulo-p (p=prime) summers, 2) amplifiers whose gains are integers $<p$, and 3) unit delays are considered. Such circuits are characterized in terms of the modular field $GF(p)$ and vectors and matrices defined thereover. A summary of the properties of $GF(p)$ is given. The use of Z transforms for linear modular sequential circuits is demonstrated. Inputs and outputs are represented by their "transforms" and the circuit by its "transfer function." The transform of the output is the product of the transfer function and the transform of the input. Several illustrative examples are included.

500
The Theory of Autonomous Linear Sequential Networks, by B. Elspas (Stanford Res. Inst.); IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 45–60; March, 1959.

Analysis and synthesis techniques for a class of sequential discrete-state networks are discussed. These networks, made up of arbitrary interconnections of unit-delay elements (or of trigger flip-flops), modulo-p adders, and scalar multipliers (modulo a, prime p), are of importance in unconventional radar and communication systems, in automatic error-correction circuits, and in the control circuits of digital computers. In addition, these networks are of theoretical significance to the study of more general sequential networks. The basic problem considered is that of finding economical realizations of such networks for prescribed autonomous (excitation-free) behavior.

501
Linear Multivalued Sequential Coding Networks, by J. Hartmanis (General Electric Res. Lab.); IRE TRANS. ON CIRCUIT THEORY, vol. CT-6, pp. 69–74; March, 1959.

Linear multivalued sequential coding networks, *i.e.*, circuits whose input and output are synchronized sequences of nonnegative integers less than some fixed number m, are discussed. The output of such networks depends linearly on the present input and a finite number of previous inputs and outputs. The transfer characteristics of such a network are described by a ratio of polynomials in the delay operator, where the multiplication and addition are performed with respect to the fixed modulus m. An algebraic theory of the delay polynomials is obtained. It is shown that a polynomial has a complete set of null sequences if, and only if, its first and last coefficients are prime to the modulus m. The polynomials with no null sequences are characterized. It is shown when common null sequences imply that the polynomials have common factors and that a complete set of null sequences defines the polynomial. It is also shown that a transfer function can be realized if the denominator contains a constant term prime to m and explicit constructions are given. A network is stable if the polynomial in the denominator of the transfer junction has no null sequence. Thus any nontrivial polynomial or its inverse is unstable if we are working modulo a prime. If the modulus is not prime, stable networks with stable inverses are constructed. Finally it is indicated how polynomials with no null sequences can be used to simplify the construction of coding networks.

502
Graph Theory and Electric Networks, by F. Harary (Princeton University and Inst. for Advanced Study); SPECIAL SUPPLEMENT TO IRE TRANS. ON CIRCUIT THEORY AND ON INFORMATION THEORY, vol. CT-6 and vol. IT-5, pp. 95–109; May, 1959.

Several topics concerning electric networks are discussed in graph theoretic terms. These are: Kirchhoff's laws, mesh and node equations, and matrix tree theorem; flow problems and Menger's theorem; Boolean functions and enumeration and synthesis problems; information theory and Markov chains; cut sets and incidence matrices; the "crummy relay" results of Moore and Shannon; and the treatment using electrical concepts of the dissections of rectangles into squares by Brooks, Smith, Stone, and Tuttle. The treatment is expository, but introduces the unifying framework of graph theory for these various considerations.

503
Classification and Minimization of Switching Functions, by N. C. de Troye (University of Amsterdam); *Philips Res. Repts.*, vol. 14, pp. 151–193, April, 1959; pp. 250–292, June, 1959.

An attempt is made to find from a given Boolean function—also called switching function because of its application in computer techniques—either the minimal sum of products or the minimal product of sums. It is demonstrated that it is possible to transform any given switching function into a matrix containing only the elements 0 or 1. The number of elements 1 in the various submatrices indicates whether a simplified notation of the switching function is possible. The possibility of easily finding the prime implicants of the switching function is likewise shown. These prime implicants can then be used to determine the minimum sum of products. It is found that this process can be carried out by means of electronic computers. The number of switching functions of n variables is 2^{2^n}. As is demonstrated, it is not necessary to determine the minimum sum of products for all these switching functions if the concept of equivalence class, *i.e.*, the set of all switching functions that are invariant as regards permutation and negation of variables, is introduced. Every equivalence class has a representative and it is only of this representative that the minimal sum of products has to be obtained. Determining the equivalence class for any given switching function of 3 or 4 variables is a relatively simple matter.

504
On the Classification of Boolean Functions, by S. W. Golomb (Jet Propulsion Lab.); SPECIAL SUPPLEMENT TO IRE TRANS. ON CIRCUIT THEORY AND ON INFORMATION THEORY, vol. CT-6 and vol. IT-5, pp. 176–186; May, 1959.

Two Boolean functions which differ only by permutation and complementation of their n input variables belong to the same symmetry class. Methods for determining the number of symmetry classes for functions of n variables, and for ascertaining whether or not two functions belong to the same class are described. This classification is achieved via a complete set of invariants, characteristic of the class, and easily computable from any function in it. The invariants also provide information concerning the size and symmetry properties of the class. Analogous techniques apply to other symmetry classifications of Boolean functions and to more general categories of discrete mappings.

505
Boolean Matrix Equations in Digital Circuit Design, by R. S. Ledley (Natl. Bur. of Standards); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 131–139; June, 1959.

A systematic digital computational method that involves the use of Boolean matrix equations for solving certain types of functional circuit design problems is given. Specifically, all sets of Boolean functions $f_1(A_1, \cdots, A_l), \cdots, f_J(A_1, \cdots, A_l)$ are found such that if circuits with these outputs are connected to a circuit that generates the known Boolean function $F(f_1, \cdots, f_J, X_1, \cdots, X_K)$, then the output will produce a given desired function $E(A_1, \cdots, A_l, X_1, \cdots, X_K)$. Illustrative examples of the method are presented.

506
Logic Matrices and the Truth Function Problem, by D. B. Netherwood (Wright Air Dev. Center); *J. Assoc. Comp. Mach.*, vol. 6, pp. 405–414; July, 1959.

An algorithm to reduce Boolean forms of the same symmetry type to a unique symmetry variant is developed. The algorithm depends on certain properties of the form-matrix and associated distance matrix, and the ordering of their rows, to within remaining degrees of freedom, which are described.

507
Dual-Polarity Logic as a Design Tool, by P. M. Kintner (Airborne Instruments Lab.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 227–228 (L); June, 1959.

The introduction of a dual-polarity logic to describe the behavior of inverting circuits such as common-emitter connected transistors is proposed. Such inversions are to be considered as physical rather than logical inversions, compatibility being achieved by changing the polarity of the logic. The resultant method, with the introduction of appropriate flow diagrams, reduces algebraic manipulation considerably.

508
The Residue Number System, by H. L. Garner (University of Michigan); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 140–147; June, 1959.

A novel number system called the residue number system is developed from the linear congruence viewpoint. The residue number

system is of particular interest because the arithmetic operations of addition, subtraction, and multiplication may be executed in the same period of time without the need for carry. The main difficulties of the residue code pertain to the determination of the relative magnitude of two residue representations and to the division process. A discussion of the arithmetic operations and the conversion process required to convert from a residue code to a weighted code is given. It is concluded that in its present state the residue code is probably not suitable for general-purpose computation but is suitable for a special class of control problems. Further research in both components and arithmetic is required if a residue code suitable for general-purpose computation is to be obtained.

509
Residues of Binary Numbers Modulo Three, by J. Rothstein (Edgerton, Germeshausen and Grier, Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, p. 229 (L); June, 1959.

A method for determining the remainder on dividing a binary number by three, without actually dividing out, is described.

E-3: MATHEMATICS—LOGIC—NUMERICAL ANALYSIS

510
An Application of Piecewise Approximations to Reliability and Statistical Design, by H. J. Gray, Jr. (Moore School of Elec. Engrg.); PROC. IRE, vol. 47, pp. 1226–1231; July, 1959.

An algorithm which makes it relatively easy to obtain the distribution of a random variable if the variable can be expressed as a weighted sum of other random variables having known distributions which can be approximated piecewise by, for example, polynomials is described.

511
Error Analysis in Floating Point Arithmetic, by J. W. Carr, III (University of North Carolina); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 10–15; May, 1959.

Upper bounds on round-off error for the basic arithmetic operations in two floating point systems are evaluated and compared. The first is the usual normalized system in which the mantissa may contain no zeros between the point and the first significant digit; the second or significant system, in which the mantissa is less than one in absolute value with no further restriction, is used to give an approximate representation of the number of significant digits in a number. The circumstances under which the one system or the other is to be preferred are discussed.

512
Stability of the Reduction of a Matrix to Almost Triangular and Triangular Forms by Elementary Similarity Transformations, by J. H. Wilkinson (Natl. Phys. Lab., Eng.); *J. Assoc. Comp. Mach.*, vol. 6, pp. 336–359; July, 1959.

Two alternative methods for reducing a general matrix to almost triangular form by means of similarity transformations are outlined. The emphasis is on numerical stability, and a method of organizing the calculations in fixed point arithmetic to keep round-off errors to a minimum is given. The further reduction from almost diagonal to diagonal form is shown to suffer from instability and hence to be valueless unless special precautions are taken.

513
Note on the Practical Computation of Proper Values, by C. T. Fike (Oak Ridge Natl. Lab.); *J. Assoc. Comp. Mach.*, vol. 6, pp. 360–362; July, 1959.

The practical difficulty of calculating the proper or eigenvalues of a matrix is dependent upon the degree of ill-conditioning of the matrix. A "condition number" giving a measure of a matrix conditioning is proposed and defined and its main properties are developed.

514
Remarks on the Practical Solution of Characteristic Value Problems, by A. Wouk (Sylvania Electric Products, Inc.); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 38–39; June, 1959.

A method of solution of boundary value problems involving a set of ordinary differential equations in terms of the analogous initial value problems is discussed. The solution takes the form of determining the roots of a determinantal equation in the characteristic values of the system.

515
A Family of Quadrature Formulas Which Achieve High Accuracy in Composite Rules, by A. Ralston (Bell Telephone Labs., Inc.); *J. Assoc. Comp. Mach.*, vol. 6, pp. 384–394; July, 1959.

Quadrature formulas are derived which achieve higher accuracy when the interval of integration is broken up into subintervals than analogous Newton-Cotes or Gaussian formulas. The higher accuracy is achieved at the cost of computing at most two extra ordinates over the whole range of integration. Since the abscissas are not equally spaced, the method is not suitable for tabular functions or hand computation, but is very convenient on a digital computer. Round-off properties of the formulas are satisfactory.

516
Solution of Ordinary Linear Differential Equations by an *N* Step Method, by J. W. Fishbach (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 31, pp. 341–342(A); May 15, 1959. PB 139 036 (Order from LC, Mi $2.70, Ph $4.80).[1]

A procedure whereby the solution of an ordinary linear differential equation may be obtained in N steps without the necessity of finding the matrix A, or its inverse, A^{-1}, is described. Since the matrix A is not required, the storage requirements are at a minimum, and the proposed method is ideally suited for high-speed digital computers. If, in the equivalent algebraic problem, the system contains more equations than unknowns, then the proposed method will yield the most probable values of the unknowns as a least squares solution. The procedure may be used for ordinary linear differential equations with constraints.

517
A Stability Criterion for Numerical Integration, by H. S. Wilf (Nuclear Development Corp. of America); *J. Assoc. Comp. Mach.*, vol. 6, pp. 363–365; July, 1959.

A necessary and sufficient condition for the absolute stability of multipoint numerical integration formulas for differential equations is given. The condition is that a certain matrix of low order, whose elements are computable from the coefficients of the integration formula, be positive definite.

518
Generation of Spherical Bessel Functions in Digital Computers, by F. J. Corbató (M.I.T.) and J. L. Uretsky (University of California); *J. Assoc. Comp. Mach.*, vol. 6, pp. 366–375; July, 1959.

A ratio method of computation, based on the use of recurrence relations, for spherical Bessel functions of real and imaginary argument is given. The method is easily applied to Legendre functions and cylindrical Bessel functions. The accuracy and convergence of the method are examined and criterion formulas are given. A procedure based on the Wronskian is used to simplify the final normalization.

519
An Algorithm for the Determination of the Polynomial of Best Minimax Approximation to a Function Defined on a Finite Point Set, by P. C. Curtis, Jr. and W. L. Frank (Space Technology Labs.); *J. Assoc. Comp. Mach.*, vol. 6, pp. 395–404; July, 1959.

An algorithm for determining the polynomial of best approximation to a function, in the minimax or Tchebycheff sense, is described. Starting from the solution of an initial arbitrary linear system, successive iterations have monotonically decreasing errors and converge in a finite number of steps to the best approximation.

520
Complex-Curve Fitting, by E. C. Levy (Space Technology Labs.); IRE TRANS. ON AUTOMATIC CONTROL, vol. AC-4, pp. 37–43; May, 1959.

The mathematical analysis of linear dynamic systems, based on experimental test results, often requires that the frequency response of the system be fitted by an algebraic expression. The form in which this expression is usually desired is that of a ratio of two frequency-dependent polynomials. A method of evaluation of the polynomial coefficients is presented. It is based on the minimization of the weighted sum of the squares of the errors between the absolute magnitudes of the actual function and the polynomial ratio, taken at various values of frequency (the independent variable). The problem of the evaluation of the unknown coefficients is reduced to that of the numerical solution of certain determinants. The elements of these determinants are

functions of the amplitude ratio and phase shift, taken at various values of frequency. This form of solution is particularly adaptable to digital computing methods because of the simplicity in the required programming. The treatment is restricted to systems which have no poles on the imaginary axis; *i.e.*, to systems having a finite, steady-state (zero frequency) magnitude.

521
Parameter Estimation for Simple Nonlinear Models, by W. M. Chow (Union Carbide Plastics); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 28–29; July, 1959.

The fitting of experimental data from the field of rheology to a nonlinear model of the form $y=a+x^m/b$ is discussed. The relative merits of various standard methods are compared, with preference given to a cubic equation modification of the Newton-Gauss method. A special procedure depending on correlation coefficients is developed.

E-4: MATHEMATICS—LOGIC—THEORETICAL LINGUISTICS

522
On Certain Formal Properties of Grammars, by N. Chomsky (M.I.T. and Inst. for Advanced Study, Princeton); *Information and Control*, vol. 2, pp. 137–167; June, 1959.

A grammar can be regarded as a device that enumerates the sentences of a language. A sequence of restrictions that limit grammars first to Turing machines, then to two types of systems from which a phase structure description of the generated language can be drawn, and finally to finite-state Markov sources (finite automata) is discussed. These restrictions are shown to be increasingly heavy in the sense that the languages that can be generated by grammars meeting a given restriction constitute a proper subset of those that can be generated by grammars meeting the preceding restriction. Various formulations of phase structure description are considered and the source of their excess generative power over finite state sources is investigated in greater detail.

523
The Use of Statistics in Language Research, by A. F. Parker-Rhodes (Cambridge Language Research Unit, Cambridge, Eng.); *Mech. Translation*, vol. 5, pp. 67–73; November, 1958.

The literature on the application of statistical methods to the problems of mechanical translation is reviewed. It is concluded that much of the work done is of little direct interest in mechanical translation, and that statistics can play a useful part only after the main procedures of mechanical translation are firmly established.

524
Some Problems in the Mechanical Translation of German, by L. Brandwood (Birkbeck College, London, Eng.); *Mech. Translation*, vol. 5, pp. 60–66; November, 1958.

Problems of syntactical ambiguity and multimeaning in the translation of relative pronouns and prepositional phrases from German into English are discussed. The problems arise from the coexistence in German of homomorphous inflections and variable word order, combined with gender dissimilarities in the two languages. Some possible or partial solutions based on a statistical analysis of such ambiguities encountered in scientific text are discussed.

525
Soviet Developments in Machine Translation: Russian Sentence Analysis, by T. M. Nikolaeva (Inst. of Precise Mechanics and Computing Technique, Moscow, U.S.S.R.); *Mech. Translation*, vol. 5, pp. 51–59; November, 1958.

The entire analysis of Russian is broken down into two independent parts: a dictionary containing a complete grammatical description of the word, and the subsequent grammatical analysis. The syntactical analysis of the Russian sentence is described, with attention given to the function of contextual environment, word order, homonymity, equivalence, and the like.

E-5: MATHEMATICS—LOGIC—INFORMATION THEORY

526
Some Inequalities Satisfied by the Quantities of Information of Fisher and Shannon, by A. J. Stam (Netherlands Defence Res. Council); *Information and Control*, vol. 2, pp. 101–112; June, 1959.

A certain analogy is found to exist between a special case of Fisher's quantity of information I and the inverse of the "entropy power" of Shannon. This can be inferred from two facts: 1) both quantities satisfy inequalities that bear a certain resemblance to each other; 2) there is an inequality connecting the two quantities. This last result constitutes a sharpening of the uncertainty relation of quantum mechanics for canonically conjugated variables. Two of these relations are used to give a direct proof of an inequality of Shannon. The proofs are not fully elaborated.

527
Functional Equations in Adaptive Processes and Random Transmission, by R. Bellman and R. Kalaba (The Rand Corp.); Special Supplement to IRE Trans. on Circuit Theory and on Information Theory, vol. CT-6 and vol. IT-5, pp. 271–282; May, 1959.

By imbedding a complex physical process under consideration with an appropriate class of processes and expressing the functional relationships among the members of the class, it is frequently possible to obtain insights into the structure of the original process which would not be feasible through consideration of that process alone. Not only may analytical expressions be obtained, but frequently computational tools are forged which make possible the exploitation of modern digital computing machines. By way of illustration, recent applications of the functional equation techniques of dynamic programming and invariant imbedding to the study of some problems arising in the theory of adaptive control processes and that of transmission through random media are discussed.

528
Variable-Length Binary Encodings, by E. N. Gilbert and E. F. Moore (Bell Telephone Labs); *Bell Sys. Tech. J.*, vol. 38, pp. 933–967; July, 1959.

A theoretical treatment of several properties which describe certain variable-length binary encodings of the sort which can be used for the storage or transmission of information is given. Some of these, such as the prefix and finite delay properties, deal with the time delay with which circuits can be built to decipher the encodings. The self-synchronizing property deals with the ability of the deciphering circuits to get in phase automatically with the enciphering circuits. Exhaustive encodings have the property that all possible sequences of binary digits can occur as messages. Alphabetical-order encodings are those for which the alphabetical order of the letters is preserved as the numerical order of the binary codes, and would be of possible value for sorting of data or consultation of files or dictionaries. Various theorems about the relationships between these properties and about their relationship to the average number of binary digits used to encode each letter of the original message are proved.

529
Group Code Equivalence and Optimum Codes, by A. B. Fontaine (IBM Corp.) and W. W. Peterson (University of Florida); Special Supplement to IRE Trans. on Circuit Theory and on Information Theory, vol. CT-6 and vol. IT-5, pp. 60–70; May, 1959.

A search for optimum group codes using the IBM 704 computer is described. Some theory of the relationship between equivalent codes used in narrowing the search is described, and the method of searching is outlined. The newly found optimum codes are listed, along with a number of counter-examples to typical conjectures on binary group codes.

530
A Note on a Result in the Theory of Code Construction, by R. C. Bose and S. S. Shrikhande (University of North Carolina); *Information and Control*, vol. 2, pp. 183–194; June, 1959.

A connection between Hadamard matrices H_{4t} and the maximal binary codes $M(4t, 2t; 8t)$, $M(4t-1, 2t; 4t)$ and $M(4t-2, 2t; 2t)$ in two symbols 0 and 1 is established. By $M(n, d; m)$ is meant a set of mn-place sequences with 0 and 1 such that the Hamming distance between any two sequences is greater than or equal to d. The structure of these maximal codes is also studied.

531
Single Error-Correcting Codes for Asymmetric Binary Channels, by W. H. Kim and C. V. Freiman (Columbia University); IRE Trans. on Information Theory, vol. IT-5, pp. 62–66; June, 1959.

Minimum weight-distance relationships and rules for generating single error-correcting codes in a highly asymmetric binary channel are given. More code characters are

generally obtained for a given character length than with codes for single error-correction in symmetric channels. Examples, including one specifying the code resulting in the highest average probability of correct transmission of equiprobable messages through a highly asymmetric channel, are given.

532
Multi-Error Correcting Codes for a Binary Asymmetric Channel, by W. H. Kim and C. V. Freiman (Columbia University); Special Supplement to IRE Trans. on Circuit Theory and on Information Theory, vol. CT-6 and vol. IT-5, pp. 71–78; May, 1959.

Codes for k-tuple 1-error correction in a binary asymmetric channel which yield more code characters than symmetrical k-tuple error-correcting codes of the same length are developed. The correction scheme is generally symbol-correcting, but may require message-correction of binary sequences whose length is approximately $(k+1)^{-1}$ that of the code characters. A double 1-error correcting code is discussed in some detail and examples of code generation and correction are included.

533
A Class of Binary Systematic Codes Correcting Errors Occurring at Random and in Bursts, by L. Calabi and H. G. Haefeli (Parke Math. Labs., Inc. and Boston College); Special Supplement to IRE Trans. on Circuit Theory and on Information Theory, vol. CT-6 and vol. IT-5, pp. 79–94; May, 1959.

The results obtained to date concerning the theoretical performance of a large class of binary systematic codes, called Hobbs' codes, which can correct random errors and/or bursts of considerable length, are presented. Practical decoding schemes are given for the codes of two subfamilies and results concerning the use of these codes with erasure channels are formulated.

534
Recurrent Codes: Easily Mechanized, Burst-Correcting, Binary Codes, by D. W. Hagelbarger (Bell Telephone Labs., Inc.); *Bell Sys. Tech. J.*, vol. 38, pp. 969–984; July, 1959.

A class of codes capable of correcting multiple errors is described. Some of these codes can be implemented with considerably less hardware than is needed for previous multiple error-correcting codes. A general method for constructing a code of redundancy $1/b$ that will correct error bursts of Kb or fewer digits (K and b integers) is shown. The logical design of the encoder and decoder, as well as the guard space requirement of good digits between bursts of errors, is described.

535
A Minimum "Ones" Binary Code for English Text, by M. H. Weik (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 31, p. 369(A); May 15, 1959. PB 136 990 (Order from LC, Mi $1.80, Ph $1.80).[1]

A binary code for English text is proposed. Use of the code results in a minimization of punch wear and punch power by taking advantage of language redundancy.

E-6: MATHEMATICS—LOGIC—LINEAR PROGRAMMING

536
A "Cookbook" Approach to Linear Programming, by C. J. Craft (Peat, Marwick, Mitchell and Co.); *Univac Rev.*, vol. 2, pp. 12–15; Summer, 1959.

The Simplex method for linear programming problems is demonstrated by means of a simple example. A basic feasible solution is obtained by introducing "slack" variables that convert inequality restrictions into equalities. At each iteration a simple algorithm determines which variable must be removed from the solution and which new variable introduced, until finally the optimum solution is obtained.

G: BIBLIOGRAPHIES

537
Bibliography of Digital Magnetic Circuits and Materials, by W. L. Morgan (Radio Corp. of America) IRE Trans. on Electronic Computers, vol. EC-8, pp. 148–158; June, 1959.

A list of about 400 references relating to magnetic memory and logic circuits is presented. The bibliography is divided into 19 sections, several of which are devoted to the physical, magnetic, and switching parameters of magnetic materials. Other parts cover the circuit and logical aspects of using magnetic cores, plates, "twistors," thin films, and transfluxors. Attention is given to the use of special memory techniques such as domain wall viscosity readout, cross-field effects, and circuits operated with RF carriers. The use of magnetic cores as half adders, gates, and shift registers is recognized in a separate section. A listing of sources of further information (conference proceedings, books, and other bibliographies) is included.

J: SUMMARIES AND REVIEWS

538
Survey of the Field of Mechanical Translation of Languages, by G. W. Reitwiesner and M. H. Weik (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 31, pp. 369–370(A); May 15, 1959. PB 151 147 (Order from OTS, $1.75.)[1]

A survey of the state of the art of mechanical translation of foreign languages by means of high-speed electronic computers is presented. The mechanical translation activities of 4 U. S. Government agencies, 6 commercial organizations, 12 educational institutions, and 4 foreign organizations are reported. The subject of mechanical translation of foreign languages by machine methods is described in terms of 1) methodology or language (*i.e.*, grammatical rules, syntactical analysis, dictionaries, flow charts, and programming), and 2) machines or equipment (*i.e.*, character sensing equipment, information storage devices, printing devices, and arithmetic or processing organs). The system performances described include the 1) All Purpose Electronic X-Ray Computer (APEXC); 2) BESM (transliteration of Russian initials for high-speed electronic computing machines); 3) Datatron; 4) IBM-650; 5) IBM-701; 6) IBM-704; 7) Johnniac; 8) Univac 1; 9) Strela; 10) special purpose computer of the University of Washington; and 11) USAF mechanical Translator Mk 1. None of the organizations active in the field expects to have the capacity to translate an arbitrarily selected text in any one field of science for at least 6 to 12 months; several are hoping to be able to perform at least crude translations within that time; and some do not expect to have working programs before at least a few years.

539
Survey of Progress and Trend of Development and Use of Automatic Data Processing in Business and Management Control Systems of the Federal Government, as of December 1957, II; *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 17–20; May, 1959.

The use of electronic equipment in data processing and management control systems within the U. S. Government is surveyed. Resulting significant savings in Treasury operations, logistics inventory control and auditing are noted, and the need for further research and development is indicated.

540
The Outlook for Computer Control in the Process Industries, by I. M. Stein (Leeds and Northrup Co.); *Computers and Automation*, vol. 8, pp. 9–14; May, 1959.

The history of automatic control of continuous processes is reviewed and a conservatively optimistic forecast is made of the future. The danger of promising too much too soon with the inevitable skeptical reaction must be avoided. Direct computer control is considered unlikely to replace indirect or "blind" control.

541
A Visit to Computation Centers in the Soviet Union, by J. W. Carr III, N. R. Scott (University of Michigan), A. J. Perlis (Carnegie Inst. Tech.), and J. E. Robertson (University of Illinois); *Commun. Assoc. Comp. Mach.*, vol. 2, pp. 8–20; June, 1959.

A general description of the state of the art in the U.S.S.R. is given and the leading Soviet computing machines are described. Topics discussed include ferrite cores, switching theory, modular number systems, capacitor storage, automatic programming, linear systems, numerical analysis, and language translation. A comparative dearth of transistor applications is noted.

542
The Computer Directory and Buyers' Guide, 1959; *Computers and Automation*, vol. 8, pp. 11–93; June, 1959.

Condensed information on a comprehensive list of organizations in any way connected with computers is presented. Organizations in the computer field are listed and a buyers' guide of computer products and services for sale or rent is given.

1959 Index to Abstracts of Current Computer Literature

This index covers abstracts which were published in the TRANSACTIONS during 1959. The abstracts, in turn, covered papers which appeared in the computer literature through July, 1959.

Subject Index

Author Index

PGEC News and Notices

Solid-State Circuits Conference

The 1960 International Solid-State Circuits Conference will be held in Philadelphia on February 10–12, 1960, at the University of Pennsylvania and the Sheraton Hotel. This is the seventh annual conference in the series sponsored by the IRE, AIEE, and the University.

The session titles indicate the high interest in computer topics:

1) Applications of Tunnel Diodes
2) Thin Magnetic Films for Logic and Memory
3) Digital Logic
4) Applications of New Devices
5) Information Storage Techniques
6) Linear Amplification and Generation
7) Microelectronic Considerations
8) Parametric Circuit Techniques.

Many of the papers from this conference will appear in full in these Transactions. A digest containing long abstracts and selected illustrations from all the papers will be available to conference registrants, and, at a price of five dollars (please make check payable to "Treasurer, Solid-State Circuits Conference,") from Mr. Henry G. Sparks, The Moore School of Electrical Engineering University of Pennsylvania, 200 South 33rd Street, Philadelphia 4, Pa.

IRE International Convention

Don't forget the dates, March 21–24, 1960, for the IRE International Convention at the Coliseum and Waldorf-Astoria Hotel in New York City. Full details in the March Proceedings of the IRE.

Ohio Symposium on Programming Methods

The Fourth Annual Symposium on Recent Advances in Programming Methods, sponsored by the Central Ohio Association for Computing Machinery, will be held on March 26, 1960, at Ohio State University in Columbus. Details of the program, and other information, may be obtained from:

R. K. Kissinger, Publicity Chairman
c/o Nationwide Insurance Companies
246 North High Street
Columbus, Ohio.

WESCON

Los Angeles is host to WESCON on August 23–26, at the Sports Arena.

Symposium on Superconductive Techniques for Computing Systems

A Symposium on Superconductive Techniques for Computing Systems will be held on May 17 and 18, 1960, sponsored by the Information Systems Branch, Office of Naval Research. The Symposium will be held in the Department of Interior Auditorium on C Street, between 18th and 19th Streets, N. W., Washington, D. C.

The purpose of this Symposium is to bring together the many scientists and engineers currently engaged in cryogenic device research in order to present a complete picture of the present status of the applications of superconductivity to computers, computing systems, and information processing devices. Invited papers emphasizing device aspects have been solicited from most of the organizations in the United States which are now involved in research of this type. Approximately 16 to 18 papers will be presented at the Symposium, including those by representatives of the following activities: Burroughs Corp., Duke University, General Electric Company, International Business Machines Corp., Lincoln Laboratory of M.I.T., Arthur D. Little, Inc., University of North Carolina, Radio Corporation of America, Rutgers University, Space Technology Laboratory, and Sperry Rand Corporation. Attendance is open to all interested technical personnel.

Further information and a preliminary Symposium program (when available) may be obtained from:

Miss Josephine Leno
Code 430A
Office of Naval Research
Washington 25, D. C.
(Phone OXford 6-6213)

1960 WJCC

The date for the 1960 WJCC (Western Joint Computer Conference) is May 3–5. The place is San Francisco.

The theme of the Conference is "Computers—Challenge of the Next Decade," and special emphasis will be placed on areas in which substantial growth and development are anticipated during the 1960's, such as language translation, data retrieval, and self-teaching systems.

Proceedings will be distributed at the Conference.

Special Computer Issue of Proceedings of the IRE

The second special Computer Issue of Proceedings of the IRE is tentatively scheduled for January, 1961, with a deadline for manuscripts at August 1, 1960. A mail call for papers will be issued to the PGEC membership in February, 1960, stating the types of papers desired for this issue. Papers are to be mailed to E. K. Gannett, Managing Editor, Proceedings of the IRE, 1 East 79 Street, New York 21, N. Y.

PGEC nonmembers who wish to receive the call for papers can be placed on the mailing list by writing to Mr. Gannett or to the editor of this special issue, Harry T. Larson, Aeronutronic Division, Ford Motor Company, Ford Road, Newport Beach, Calif.

JOINT COMPUTER COMMITTEE

JCC SENEWS

SCIENCE EDUCATION SUBCOMMITTEE NEWSLETTER

Vol. 2 No. 3 December, 1959

The contents of this issue are devoted solely to the binary adder and subtracter which was presented at the 1959 Western Joint Computer Conference. It is one of the best examples of student work we have seen, and I feel certain that it should be of great use to other students and instructors. The schematic for this machine is not published here because of its size, but is available, free of charge, as a JCC Educational project.

The following is quoted from *Electronic News*, August 20, 1959. Time did not permit a personal investigation prior to publishing this issue, and it seems of sufficient importance to duplicate here.

> A small, practical digital computer designed for high school class rooms and expected to sell for less than $1000 is now being developed in the laboratories of the electrical engineering department of the University of New Mexico, here.
>
> The department has received a $20,000 grant from the National Science Foundation for the project which is under the supervision of Dr. Richard K. Moore, department chairman, and Dr. Arnold H. Koschmann, according to school officials.
>
> Dr. Moore said he believes a relatively slow but simple computer with "a memory large enough to store a short program and the numbers associated with it" can be developed to sell to schools for $500 to $1000 . . . .

We will report further on this project as information becomes available.

MICHAEL WARSHAW, *Chairman*
JCC Science Education Subcommittee
The RAND Corporation
1700 Main Street
Santa Monica, Calif.

A BINARY COMPUTER

INTRODUCTION

The binary computer described here was primarily designed as a classroom aid for teaching basic computer theory, principles of the binary number system, and practical application of physics. It was designed and constructed in conjunction with a special course on IBM 650 computers given at the Livermore High School.

This machine can perform the operations of algebraic addition and subtraction. It is a strictly relay computer and uses binary arithmetic as the basis for its operation. It has two inputs, A and B, of four bits of information for each input. Its capacity is therefore limited to the addition and subtraction of numbers up to and including 15. It was thought that a machine of larger capacity would be of no practical value as it would only be a continuation of the basic design and theory found in this machine.

The control panel of the computer consists of 1) a switch and indicator light for each bit of information in the two inputs, 2) a sign switch for each of the two inputs, 3) an operation switch indicating either addition or subtraction, and 4) an output in the form of seven lights, five to display the numerical answer and two to indicate the sign of the answer.

For the purpose of a simpler explanation, the discussion of the theory of this machine will be broken down into three parts: addition, subtraction, and sign logic.

ADDITION

Addition is performed in the most important part of the machine, the adder. There are four stages in the adder for each bit, and each stage acts independently from the rest. Three pieces of information are fed to each stage, A_i, B_i and C_{i-1}. A_i and B_i are the binary bits from the ith position of the input numbers A and B. C_{i-1} is the carry bit from the previous stage. The light in the output will be lit if any one or all three are present; it will not be lit if any two or none are present. A carry into the next ($i+1$st) stage will be effected by the presence of any two or all three inputs. Figs. 1 and 2 show how this is accomplished electrically. A carry from the fourth stage will automatically activate the fifth light in the output when the machine is doing the operation of addition.

SUBTRACTION

Subtraction in this machine is done by addition. If the machine is told that it is to do a subtract operation, it complements the B input (a process equivalent to

changing the "1's" and "0's" and vice versa). Fig. 3 shows how this is accomplished in the machine. The complemented B input is then added to the A input in the adder. The output of the adder is then analyzed to see if there is a carry from the fourth stage, as shown in Fig. 4. If there is no carry, the output is recomplemented and displayed. If, however, there is a carry, one must be added to the adder output before it is displayed, and no recomplementation is required. This is achieved by treating the addition of one as a carry from the "previous stage" into the first stage. During a subtract operation the fifth light in the output is automatically suppressed.

Sign Logic

This machine has the additional feature of sign logic which enables it to do algebraic addition or subtraction. First the machine analyzes the signs of A and B and the operation switch to determine whether it must perform an ADD or SUBTRACT operation of the absolute values. The truth table for this logic is shown in Fig. 5, and the method of implementing the logic is shown in Fig. 6.

The determination of the sign of the output is very interesting. If the machine is doing an ADD operation, the output will carry the sign of the A input. If it is doing a SUBTRACT operation, it will use the sign of the number with the largest absolute value. The problem of comparing absolute values now arises. Fortunately, a simpler device may be used. The machine will only recomplement when the absolute value of the B input is larger than that of the A input. Thus, the sign of A is used for the output at times other than when the machine recomplements, in which case the sign of B is used. Another problem arises when the operation switch is in the subtract position, the machine is performing a subtract operation, and it recomplements. In this case, the sign of B is invalid, and the opposite sign must be used to make the output sign correct. Fig. 7 shows how this is accomplished electrically.

A. Ross Harrower
John T. Doyen
Livermore Union High School
Livermore, Calif

JCC Science Education Literature

Projects

[1] Decimal to Binary Converter No. 1 (Schematic only).
[2] Decimal to Binary Converter No. 2 (Schematic only).
[3] A Paper Computer, PAPAC-OO—R. P. Mayer
[4] Binary Computer (performs algebraic addition and subtraction with display).

Articles

[1] M. Warshaw, "How Computers Work."
[2] G. E. Forsythe, "Bibliography on High School Mathematics Education."
[3] William G. Schmidt, "Boolean Algebra and the Digital Computer."

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INFORMATION FOR AUTHORS

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS is published quarterly, in March, June, September, and December, with a distribution of over 8500 copies, largely to engineers, logicians, and supervisors in the computer field. Its scope includes the design, theory, and practice of electronic computers and data-processing machines, digital and analog, and parts of certain related disciplines such as switching theory and pulse circuits.

If a paper of widespread interest beyond the computer field is submitted, it will be recommended to the Editor of PROCEEDINGS OF THE IRE for publication. If our reviewers feel that a paper should be submitted to a different IRE TRANSACTIONS, we will so recommend to the author.

Publication time in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, from receipt of the original manuscript to mailing of the issue, is normally in excess of five months, but can be made as little as 3½ months if the occasion demands and the manuscript is carefully prepared.

To avoid delay, please be guided by the following suggestions:

A. Process for Submission of a Technical Paper

1) Send to the Editor three copies of your manuscript, each copy complete with illustrations. (For Letters to the Editor, two copies will do.)

2) Enclose originals for the illustrations, in the style described below. Alternatively, be ready to send the originals immediately upon acceptance of the paper.

3) Enclose a separate sheet giving your preferred address for correspondence and return of proofs.

4) Enclose a technical biography and photograph of each author, or be ready to supply these upon acceptance of the paper. For biography style, see any IRE journal.

5) If the manuscript has been presented, published, or submitted for publication elsewhere, please so inform the Editor. Our primary objective is to publish technical material not available elsewhere, but on occasion we publish papers of unusual merit that have appeared or will appear before other audiences.

B. Style for Manuscript

1) Typewrite, double or 1½ space; use one side of sheet only. (Good office-duplicated copies are acceptable.)

2) Provide an informative 100- to 250-word summary (abstract) at the head of the manuscript. It will appear with the paper and also separately in PROCEEDINGS OF THE IRE.

3) Provide a separate double-spaced sheet listing all footnotes, beginning with "*Manuscript received by the PGEC _____," and "†(Affiliation of author)," and continuing with numbered references. Acknowledgment of financial support is often placed at the end of the asterisk footnote.

4) Give complete references, insofar as possible. See footnotes in this or previous issues for examples of IRE style. References will be printed as footnotes in the column where first mentioned.

5) You may choose to provide a "Bibliography" at the end of the paper, with items referred to by a numeral in square brackets, *e.g.*, [12], to supplement or supplant footnote references.

6) Provide a separate sheet listing all figure captions, in proper style for the typesetter, *e.g.*: "Fig. 1—Example of a disjoint and distraught manifold."

C. Style for Illustrations

1) Originals for illustrations should be sharp, noise-free, and of good contrast. We regret that we cannot provide drafting or art service.

2) Line drawings should be in India ink on drafting cloth, paper, or board. Use 8½×11 inch size sheets if possible, to simplify handling of the manuscript.

3) On graphs, show only the coordinate axes, or at most the major grid lines, to avoid a dense, hard-to-read result.

4) All lettering should be large enough to permit legible reduction of the figure to column width, perhaps as much as 4:1.

5) Photographs should be glossy prints, of good contrast and gradation, and any reasonable size.

6) Number each original on the back, or at the bottom of the front.

7) Note item B-6 above. Captions lettered on figures will be blocked out in reproduction, in favor of typeset captions.

Mail all manuscripts to:

Dr. Howard E. Tompkins, *Editor*
IRE TRANSACTIONS ON ELECTRONIC COMPUTERS
The Moore School of E.E., University of Pennsylvania
200 South 33rd Street
Philadelphia 4, Pa.